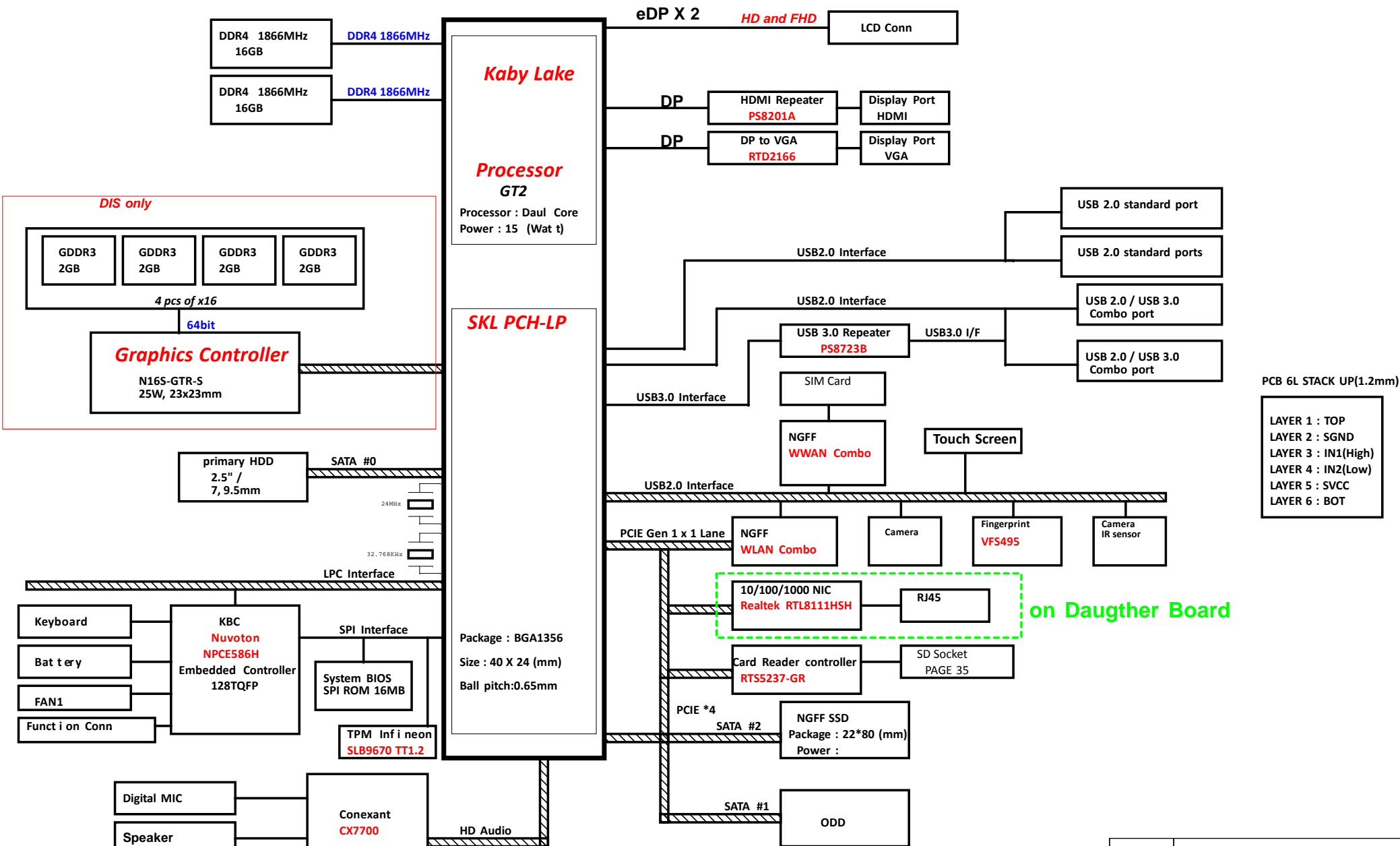
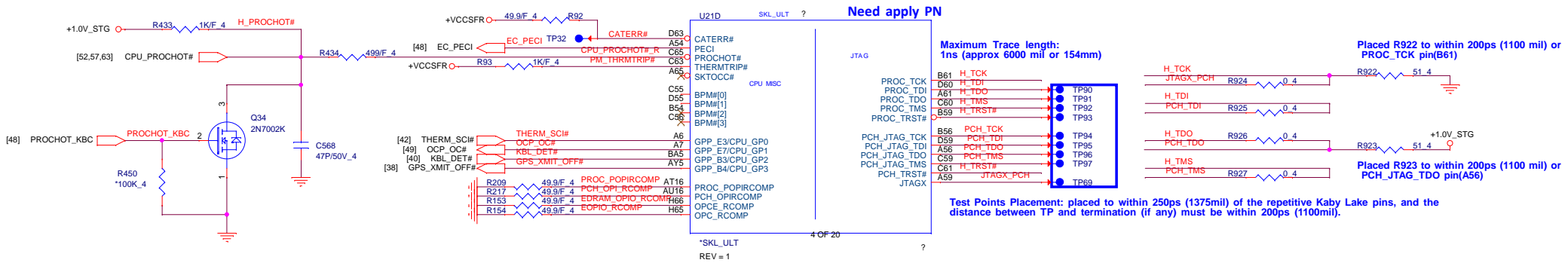
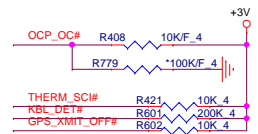


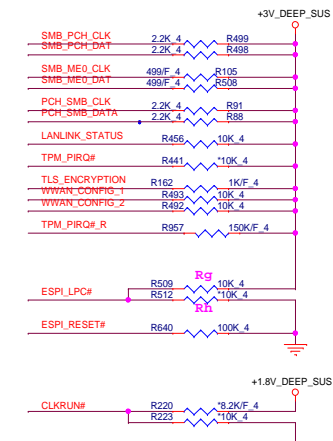
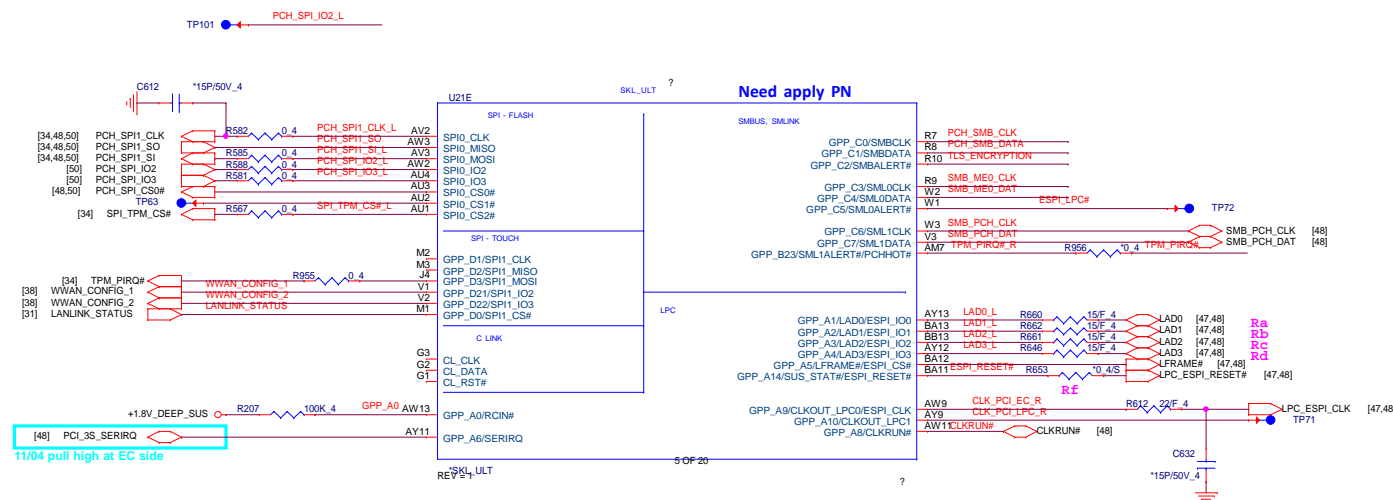
2015 400 series Kaby Lake 15"/ 17" (UMA/DIS) Block Diagram 01





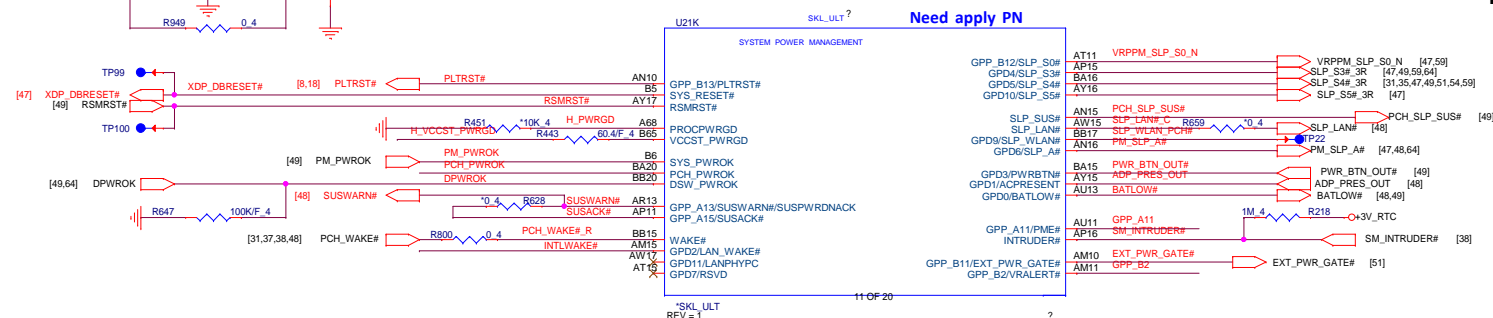
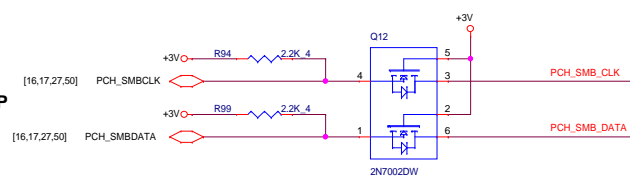
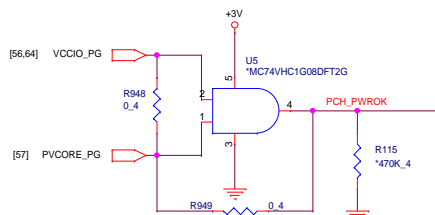
Processor pull-up (CPU)



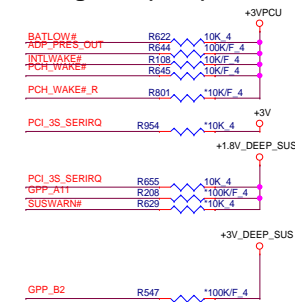


LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R660	0Ω	15Ω
R662	0Ω	15Ω
R661	0Ω	15Ω
R646	0Ω	15Ω
R653	UNINSTAL	INSTAL
R509	UNINSTAL	INSTAL
R512	INSTAL	UNINSTAL

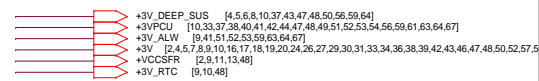
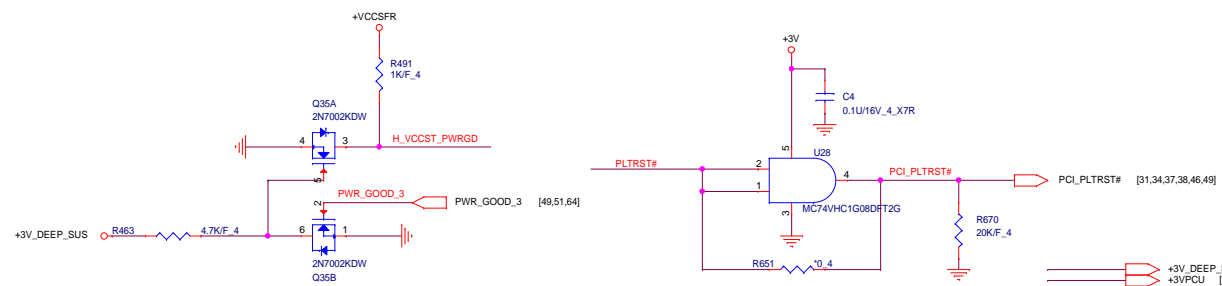
DDR/DRAM/GPU/XDP

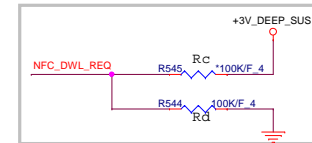
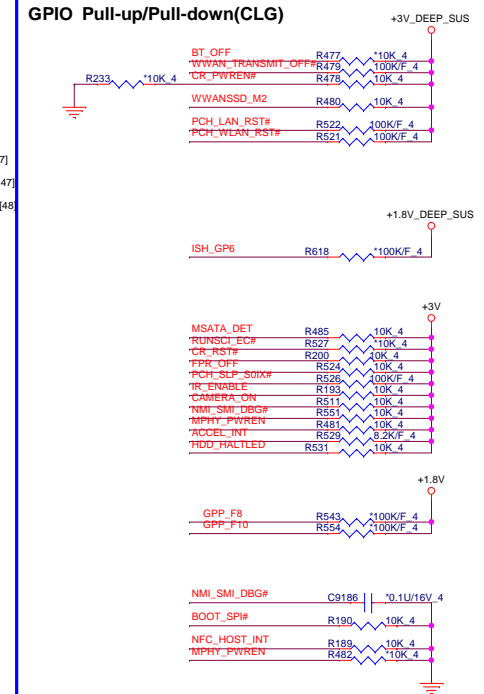
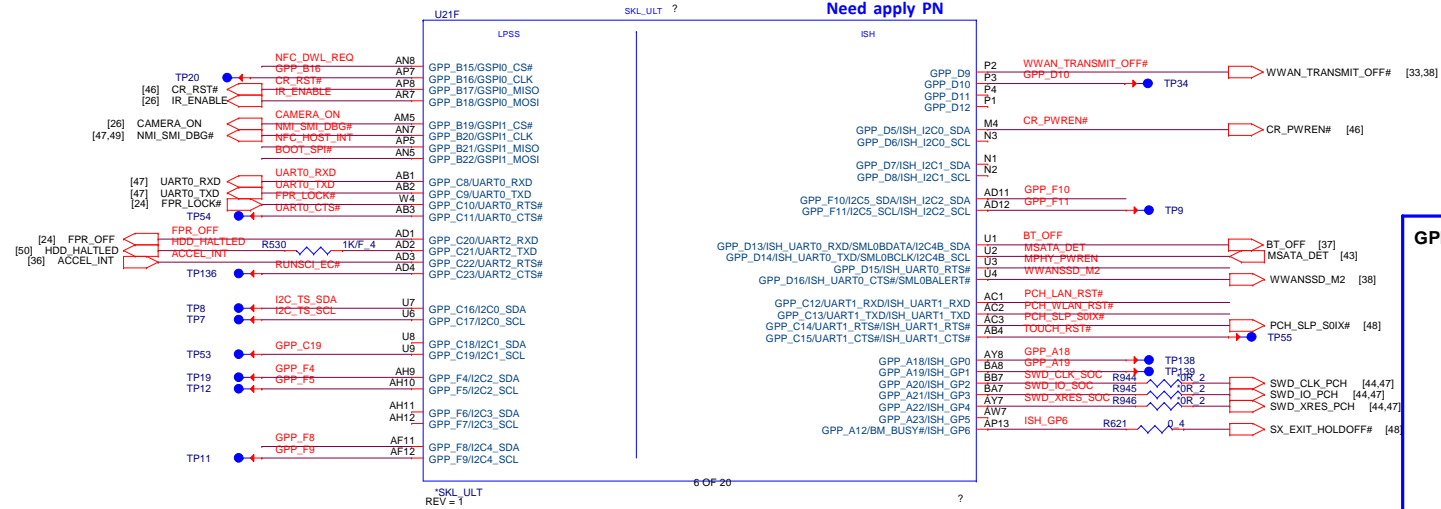


PCH Pull-high/low(CLG)

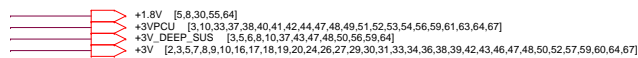


System PWR_OK(CLG)





Conexant CX7501 & CX7700 TABLE (SI stage)		
	CX7501	CX7700
Rc	UNINSTALL	INSTALL
Rd	INSTALL	UNINSTALL



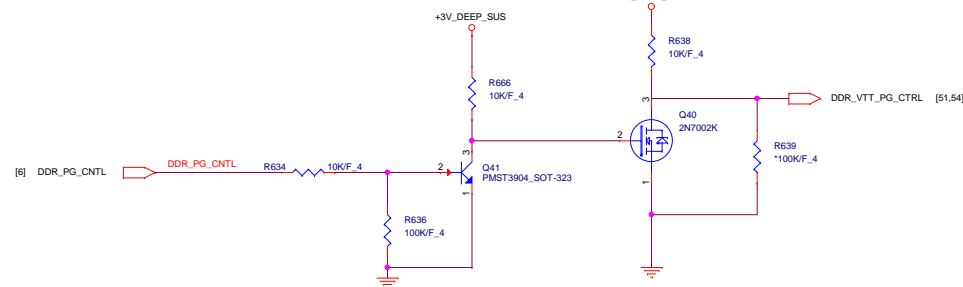
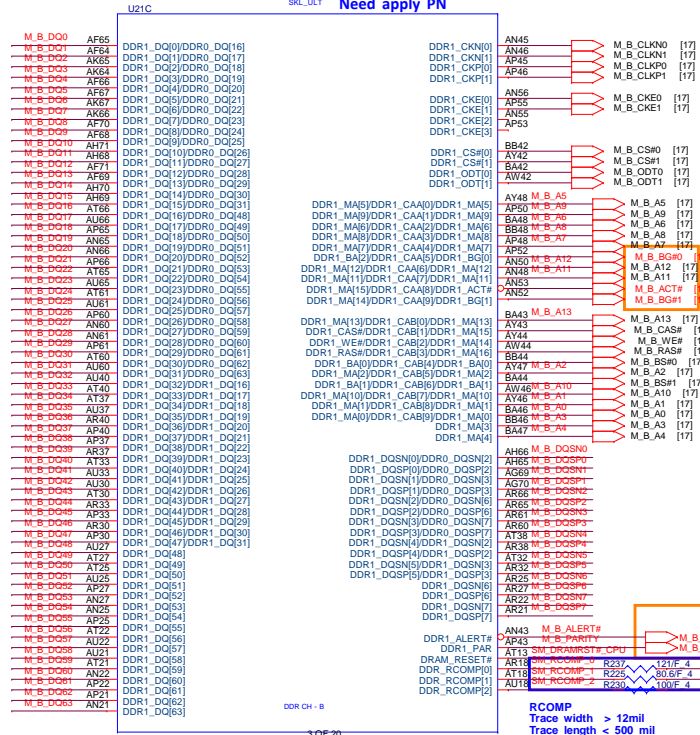
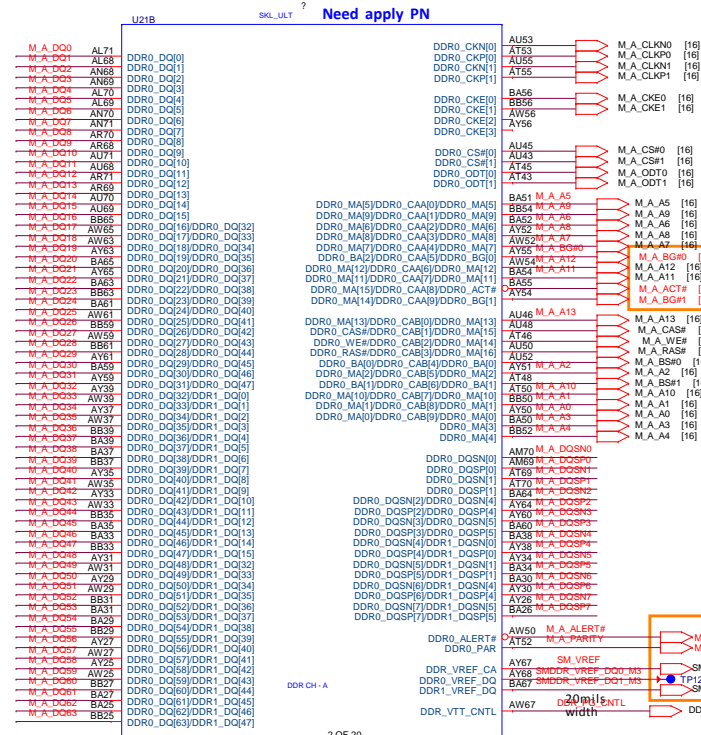
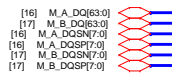
A

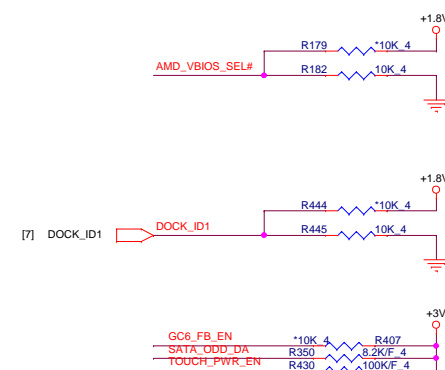
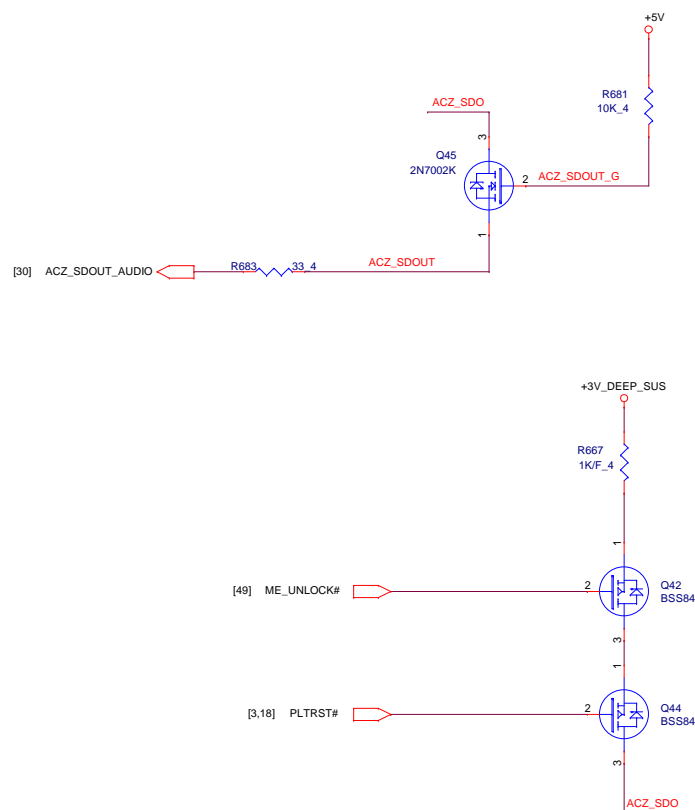
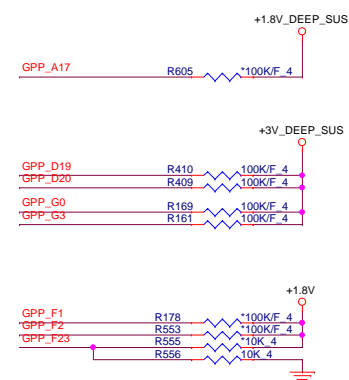
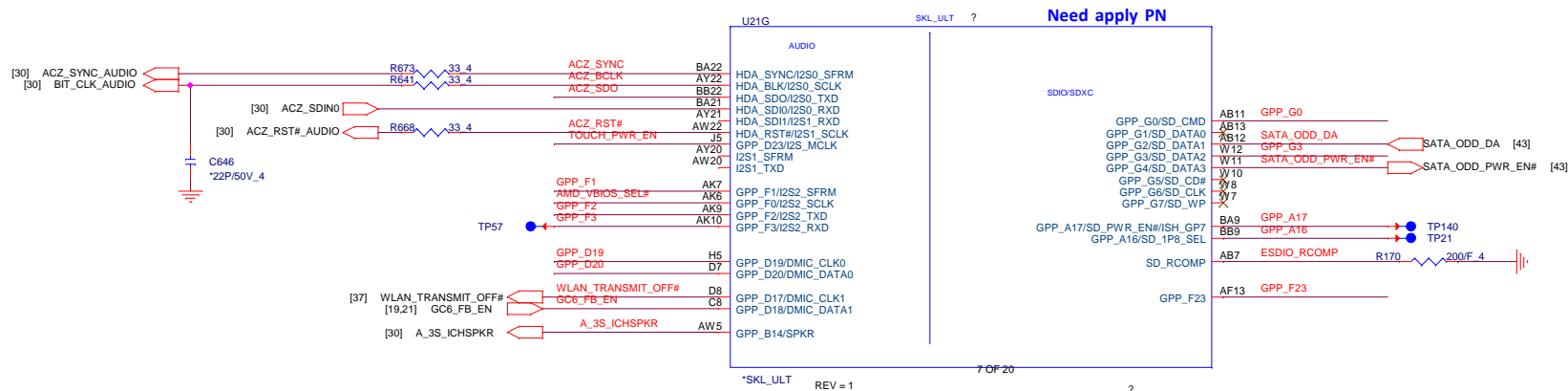
Cable detect

C

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

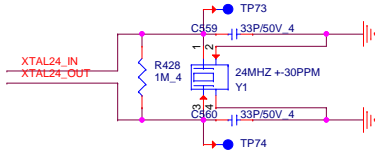
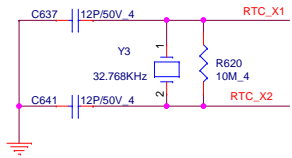
SkyLake ULT Processor (DDR4)



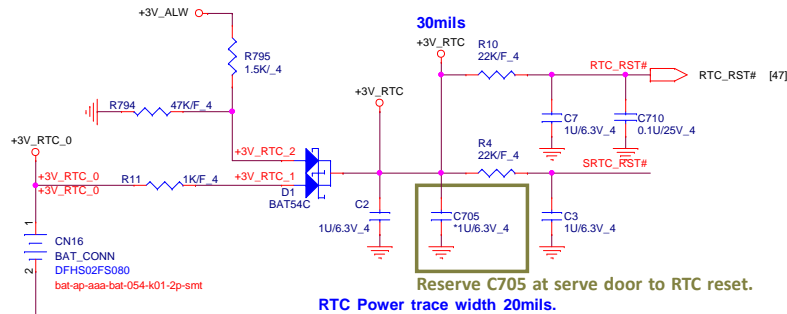


AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	

RTC Clock 32.768KHz



RTC Circuitry(RTC)

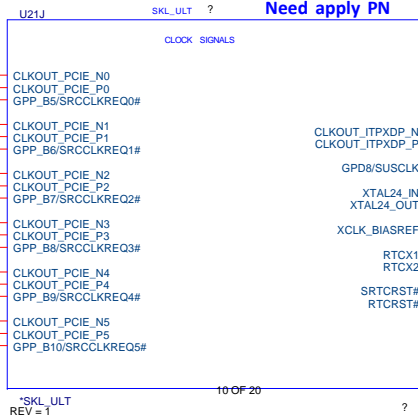
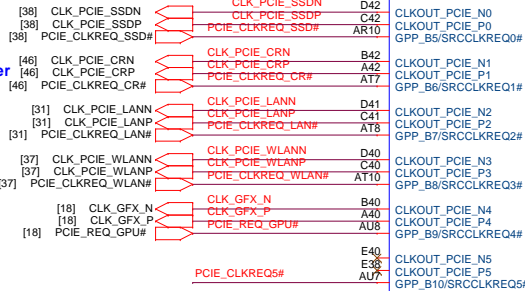


Reserve C705 at serve door to RTC reset.
RTC Power trace width 20mils.

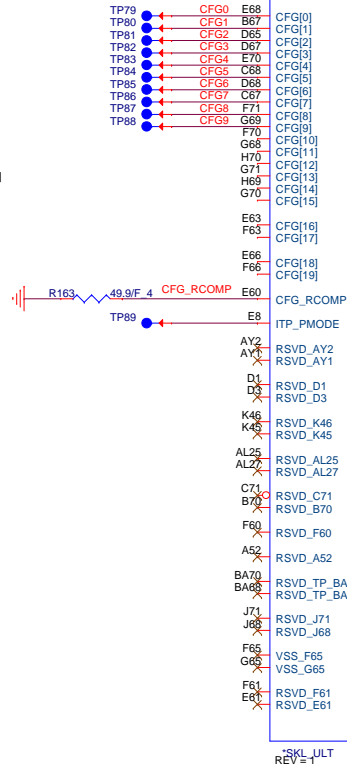


+1.0V_DEEP_SUS [10,55,56,59]
+VCC5FR [2,3,11,13,48]
+3V [2,3,4,5,7,8,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]

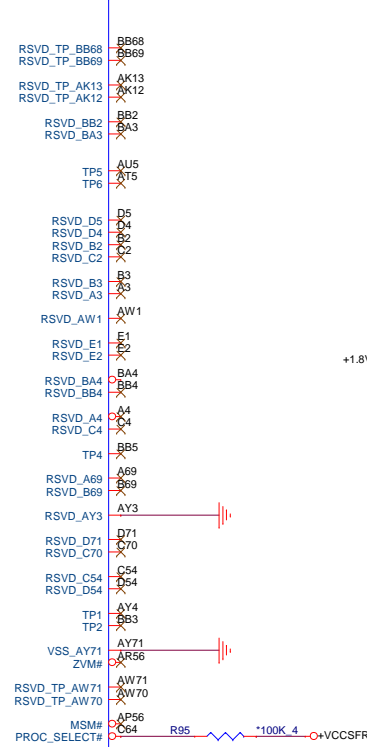
SSD
Cardreader
LAN
WLAN
dGPU



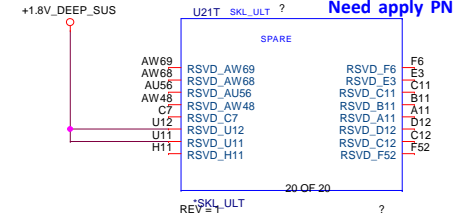
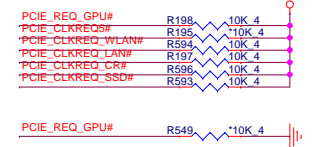
CFG0-19 need Reserve TP

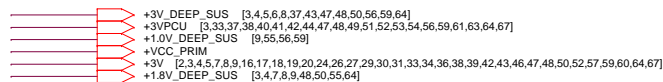
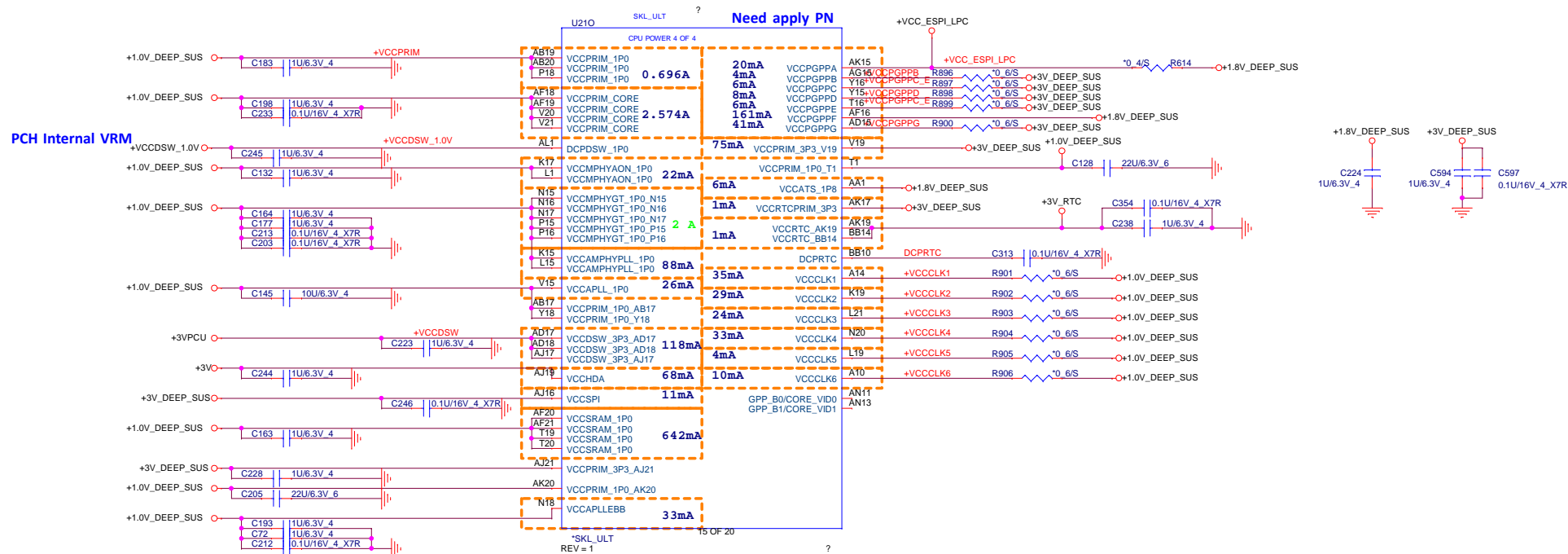


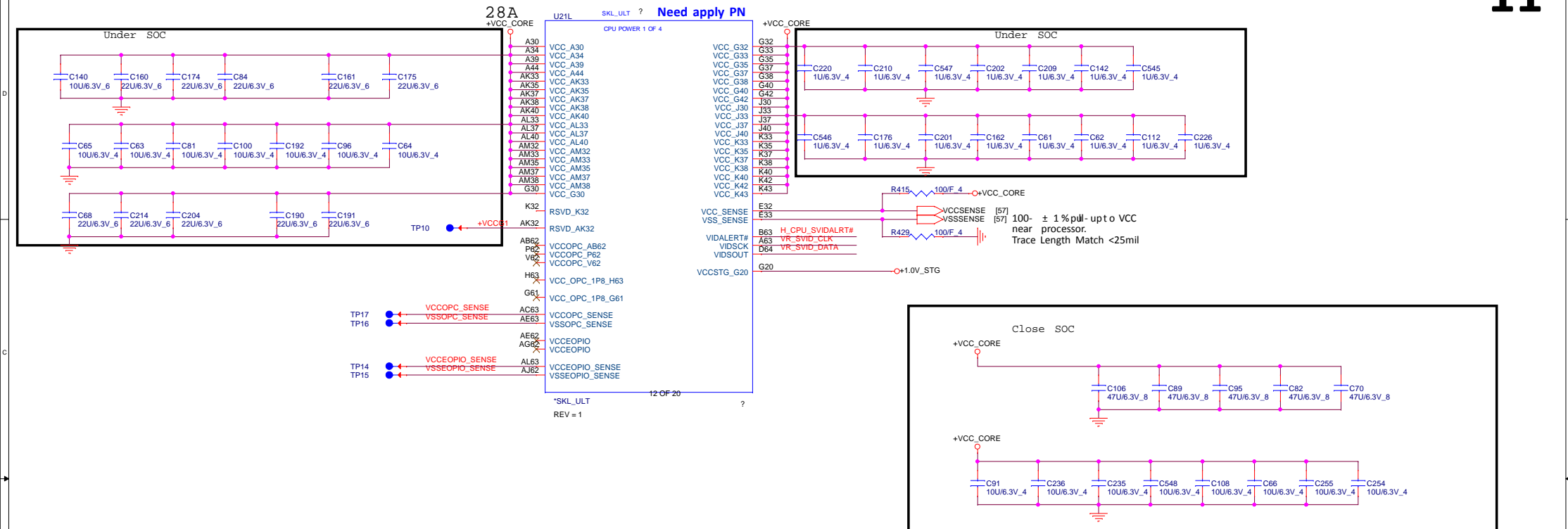
Need apply PN



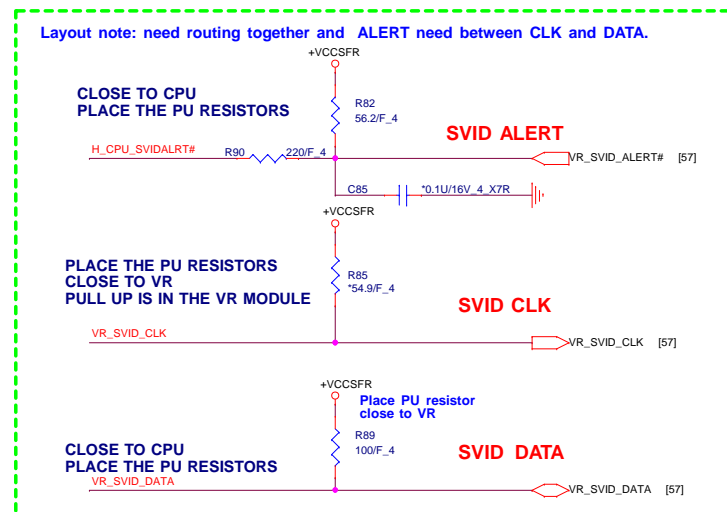
CLK_REQ/Strap Pin(CLG)



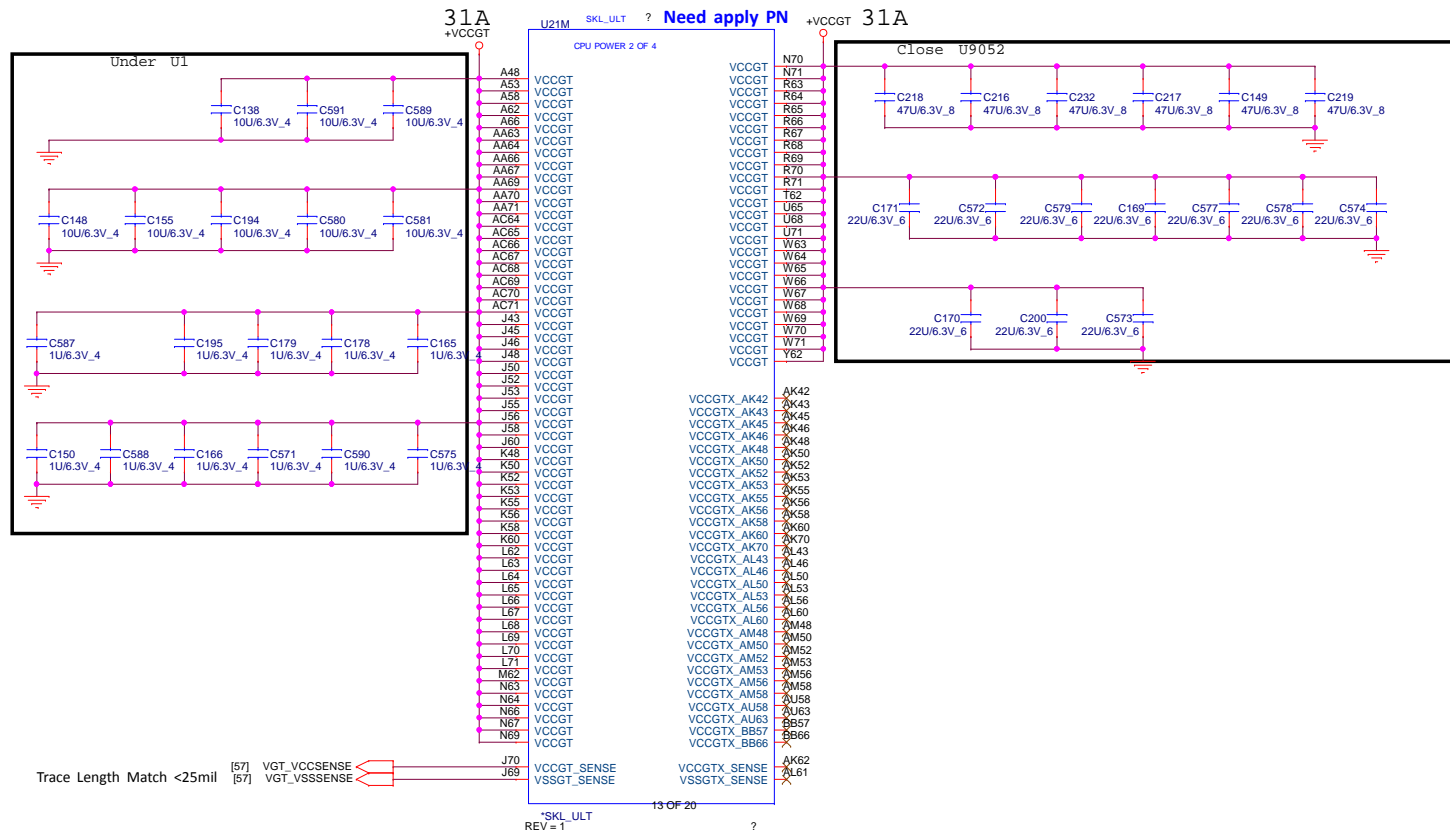




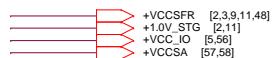
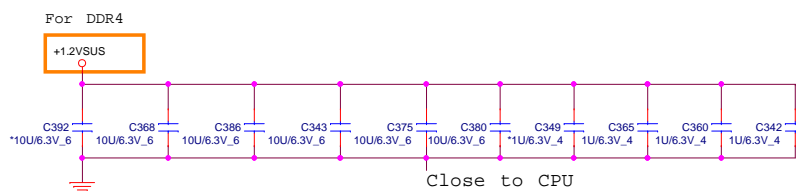
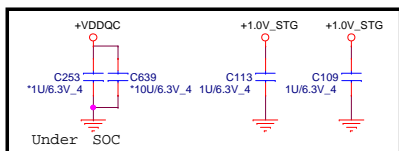
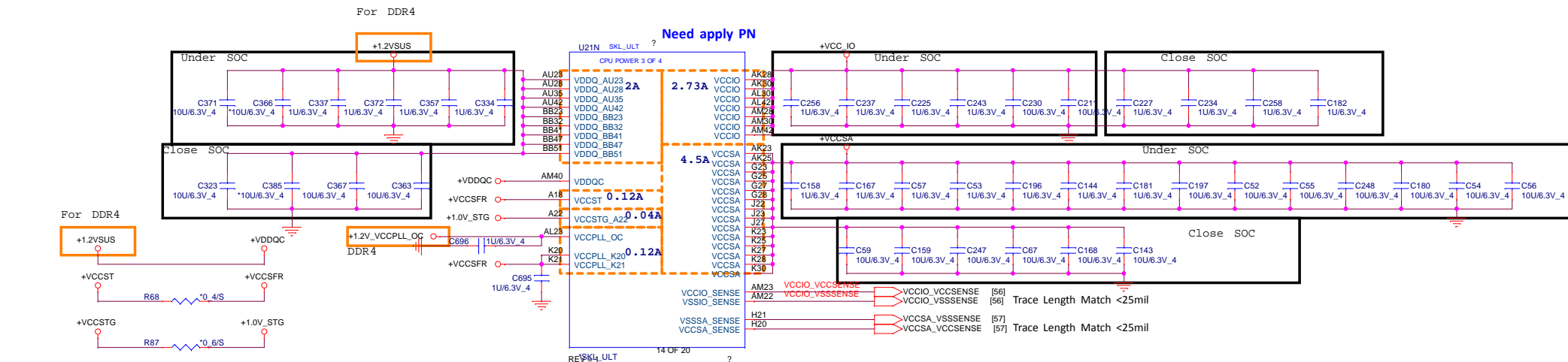
Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



+1.8V [4,5,8,30,55,64]
+VCC_CORE [57]
+VCCSFR [2,3,9,13,48]
+1.0V_STG [2,13]



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



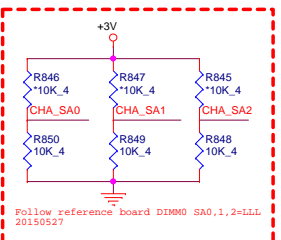
Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
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V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCeOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

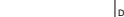
10/28 Del XDP

11/03 Del XDP

PV, 0421 Delete APS Connector

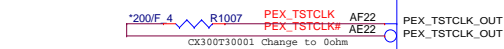
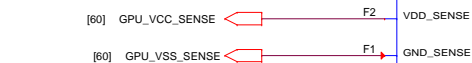
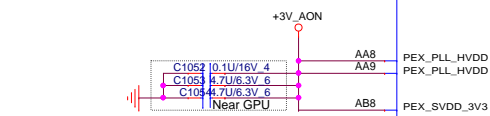
11/03 Del XDP



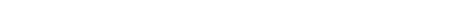
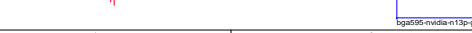
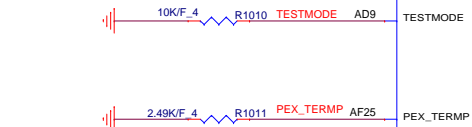


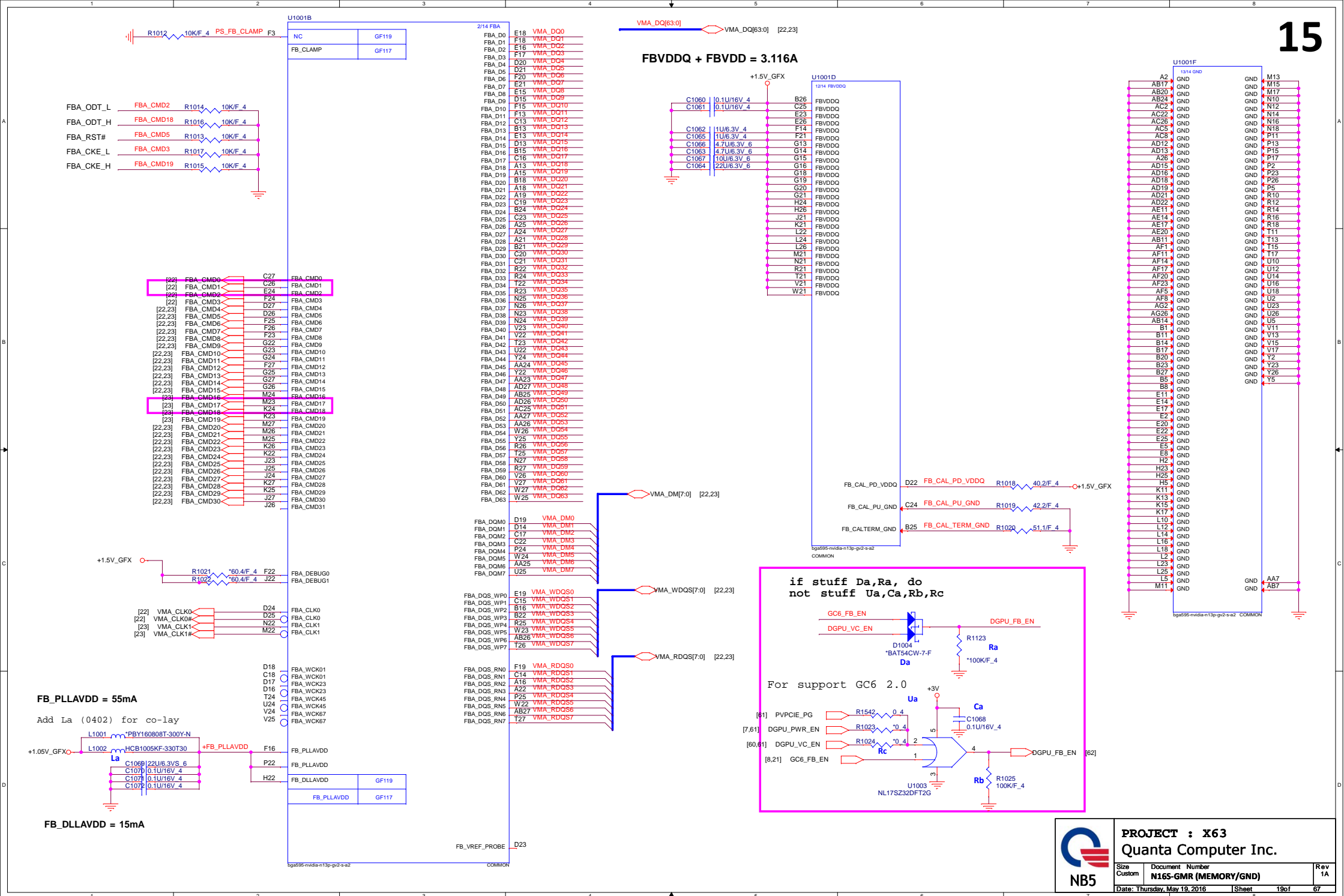
PEX_IOVDD + PEX_IOVDDQ = 1.042A

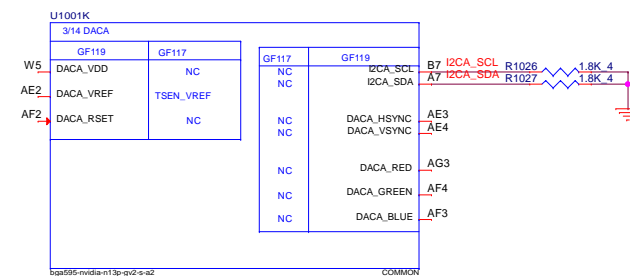
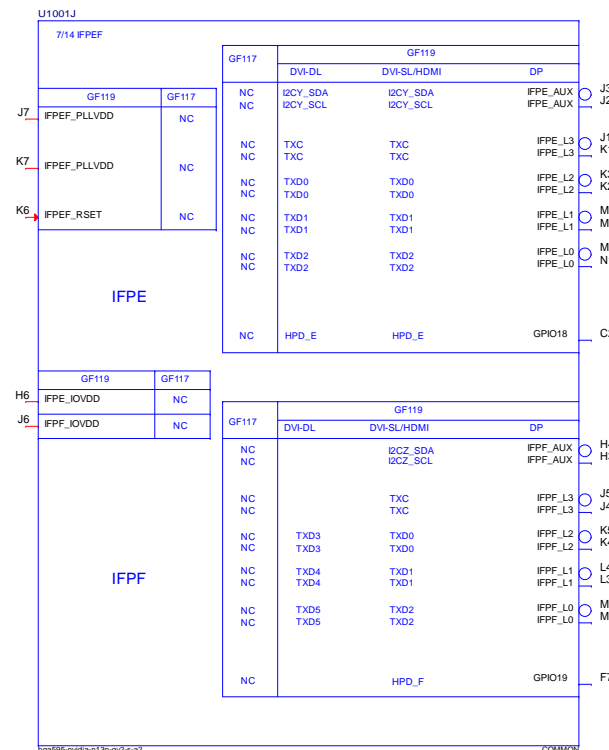
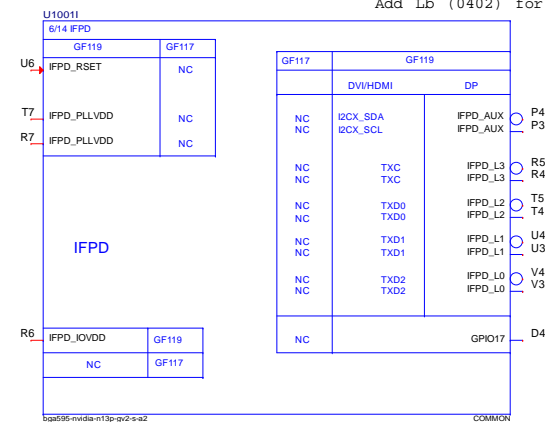
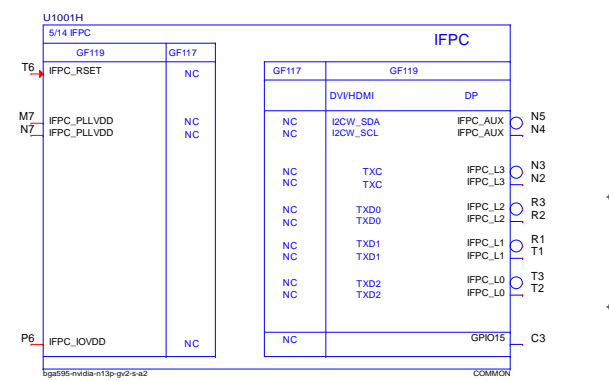
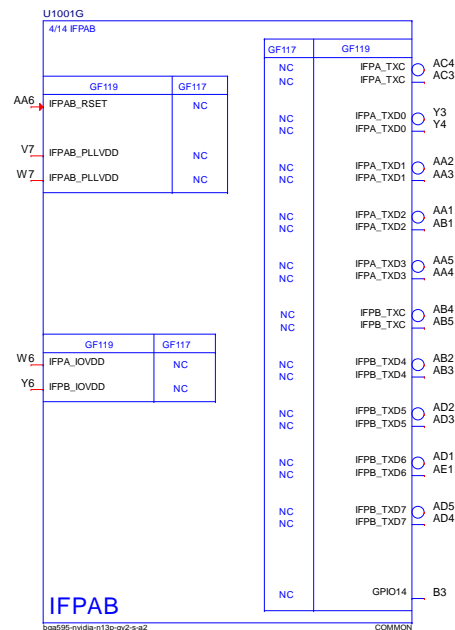
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA



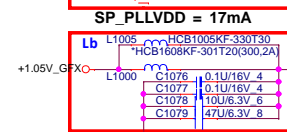
PEX_PLLVDD = 130mA



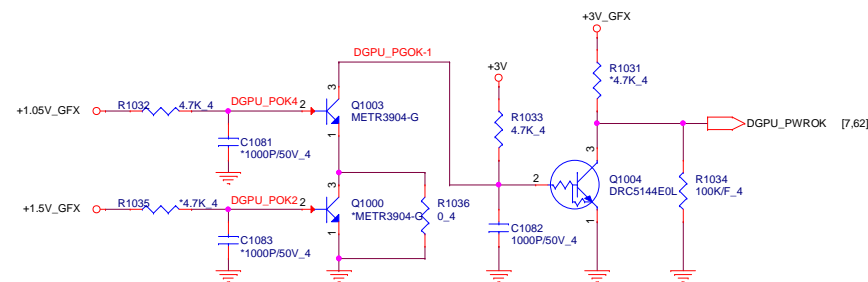
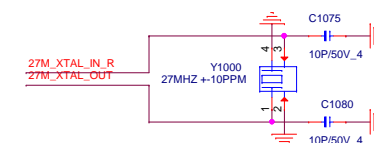




PLLVD = 38mA Add La (0402) for co-lay



VID_PLLVDD = 41mA



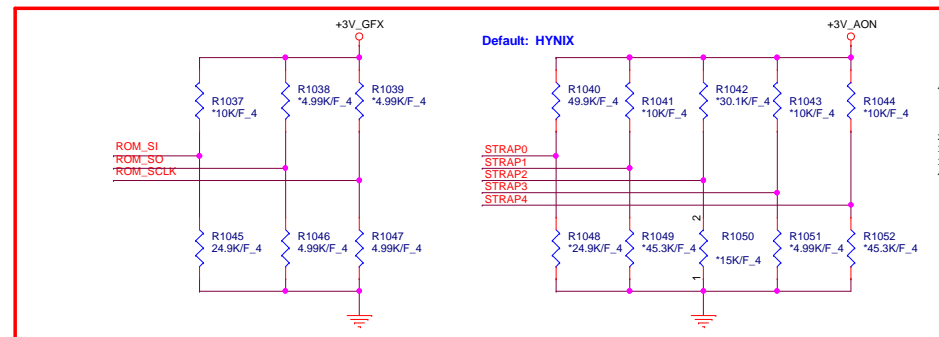
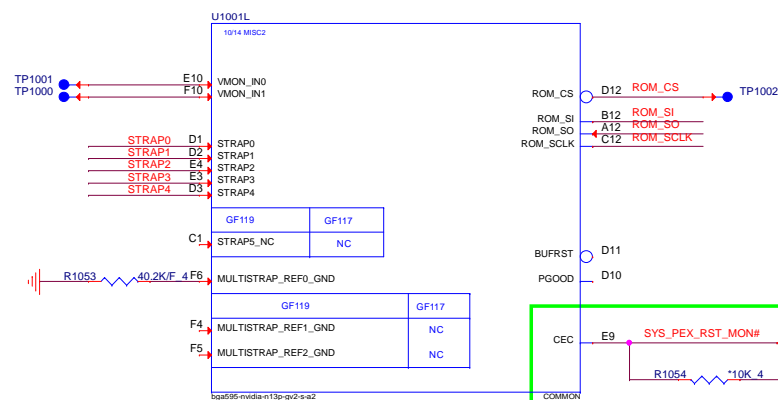
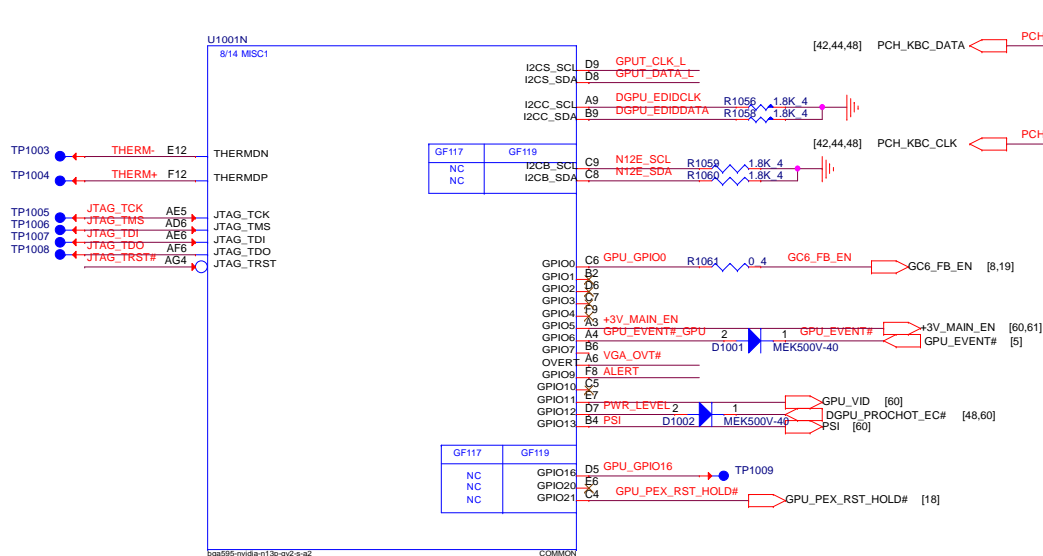


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

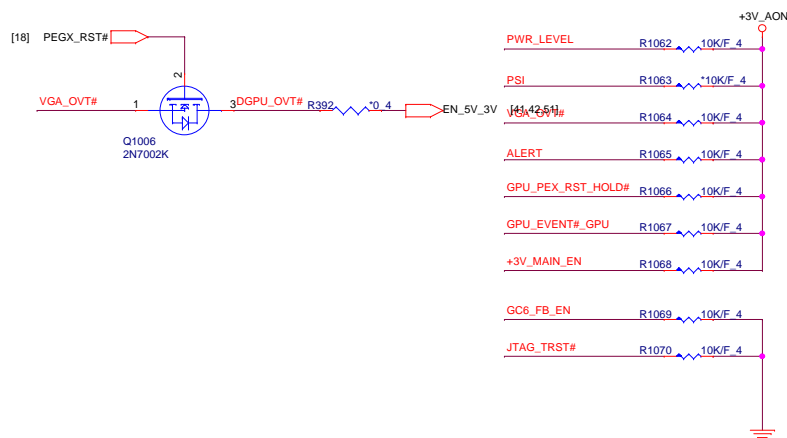


VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	Straping	TOP B/S	QBC
0000	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0101	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59G8T11	AKD59G8T100
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646B-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

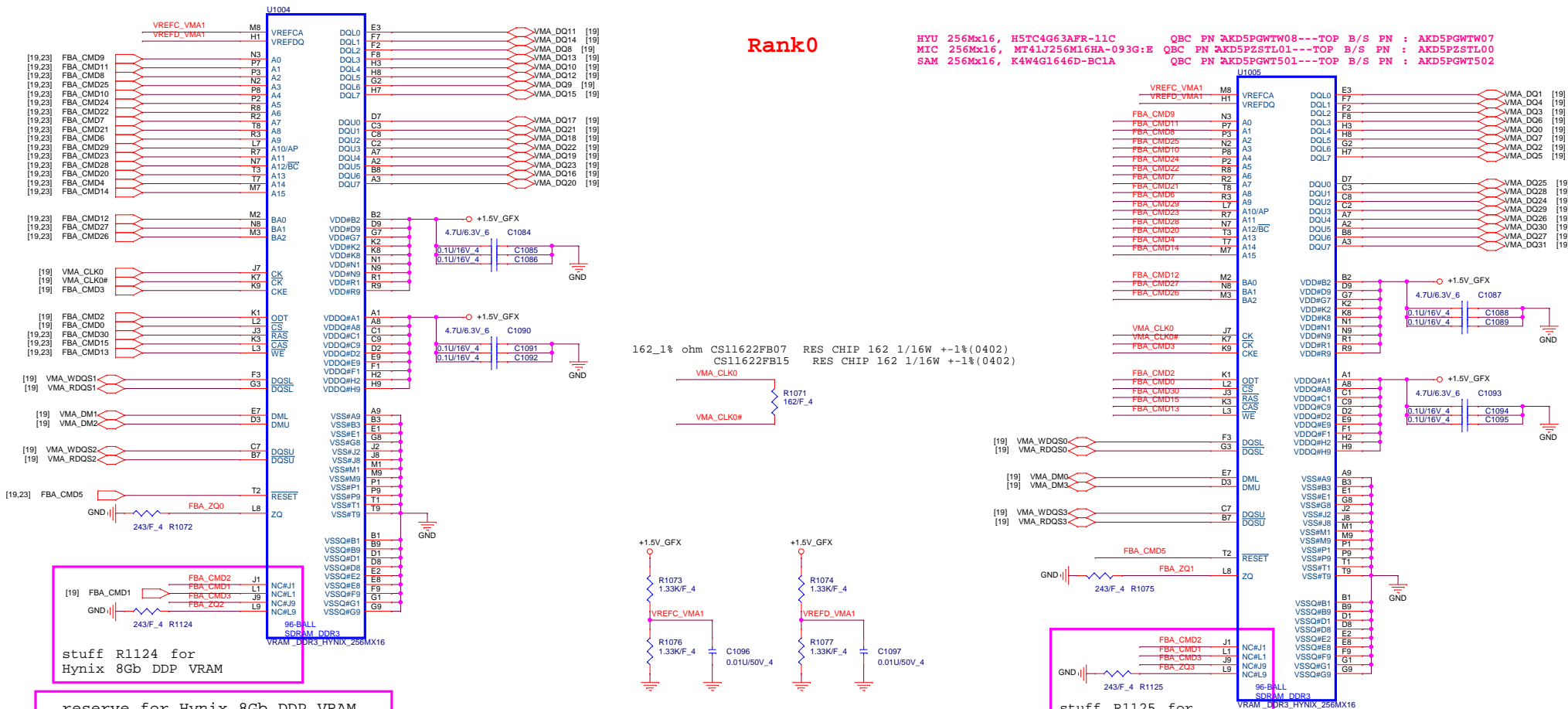
GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
 MIC 256Mx16, MT41J256M16HA-093G:E QBC PN AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
 SAM 256Mx16, K4W4G1646D-BC1A QBC PN AKD5PGWT501---TOP B/S PN : AKD5PGWT502



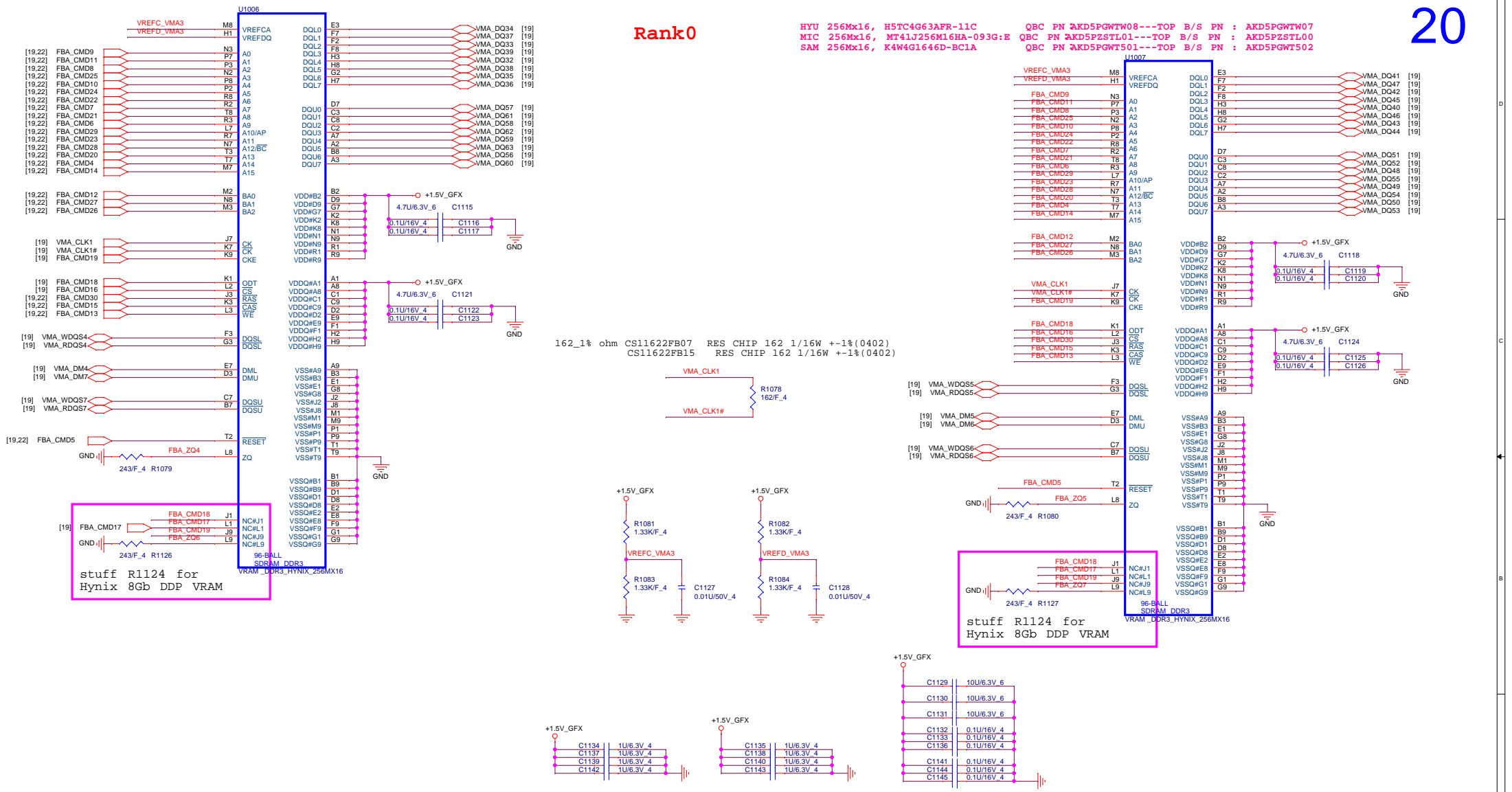
PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L - RANK0	1A
Date: Thursday, May 19, 2016	1 Sheet	22 of 67

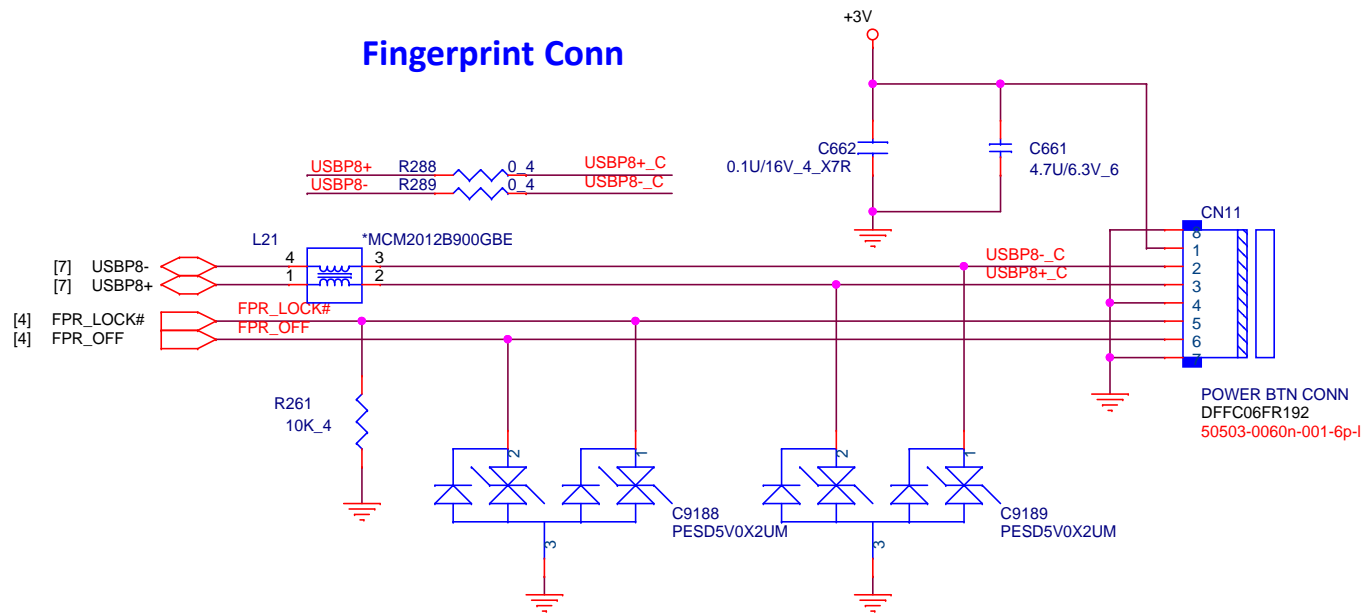
Rank0

HYU 256Mx16, H5TC4G63APR-11C
MIC 256Mx16, MT41J256M16HA-093G:E
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
QBC PN AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
QBC PN AKD5PGWT501---TOP B/S PN : AKD5PGWT502



Fingerprint Conn



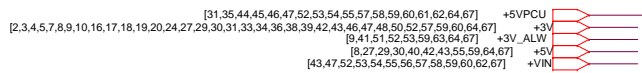
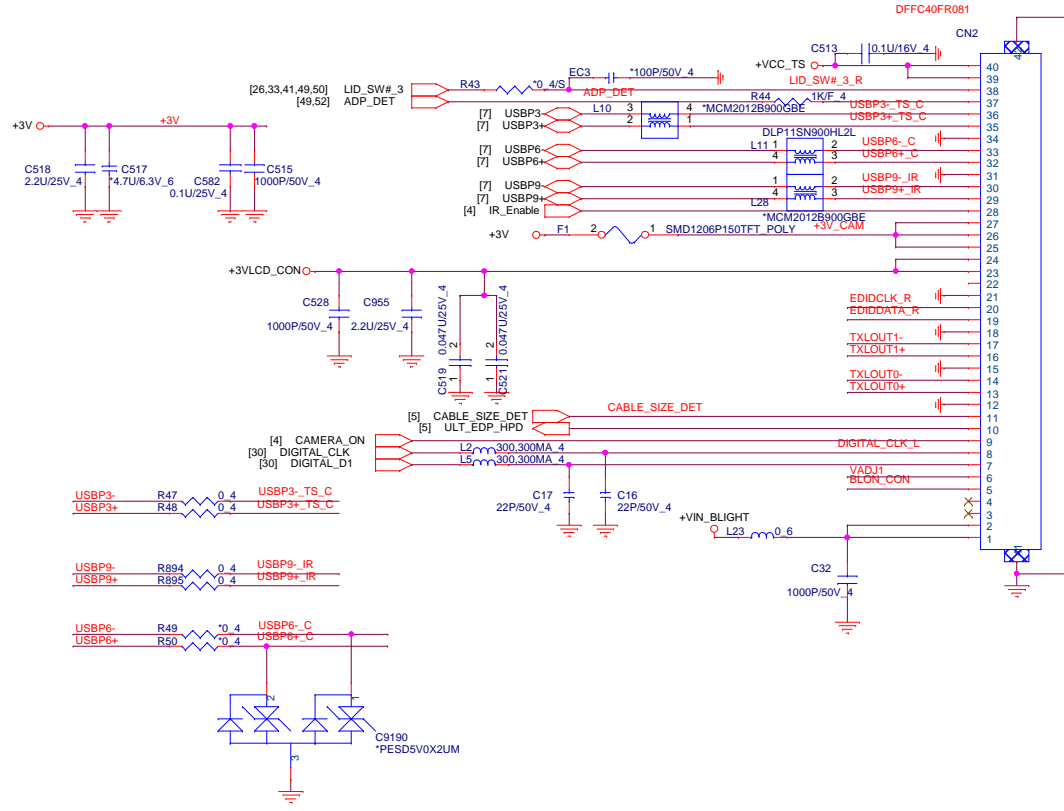
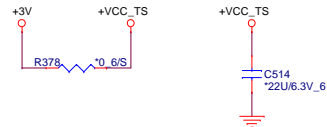
ALF@1119:
HP confir med to re move the eDP to LVDS convert α.

[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V

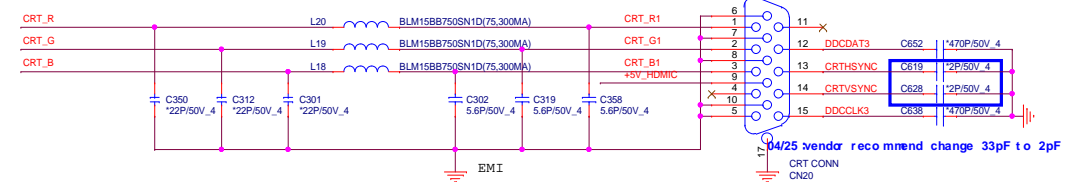
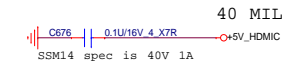
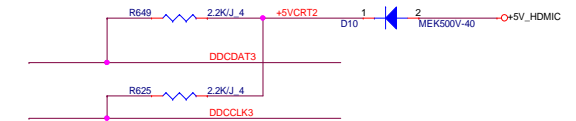
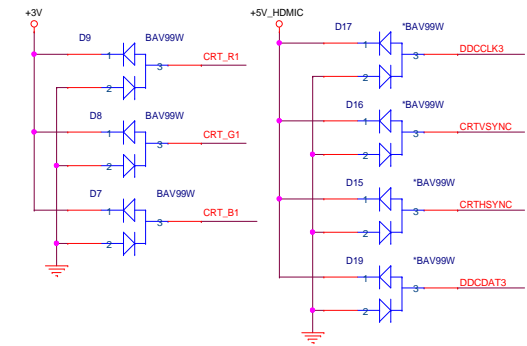
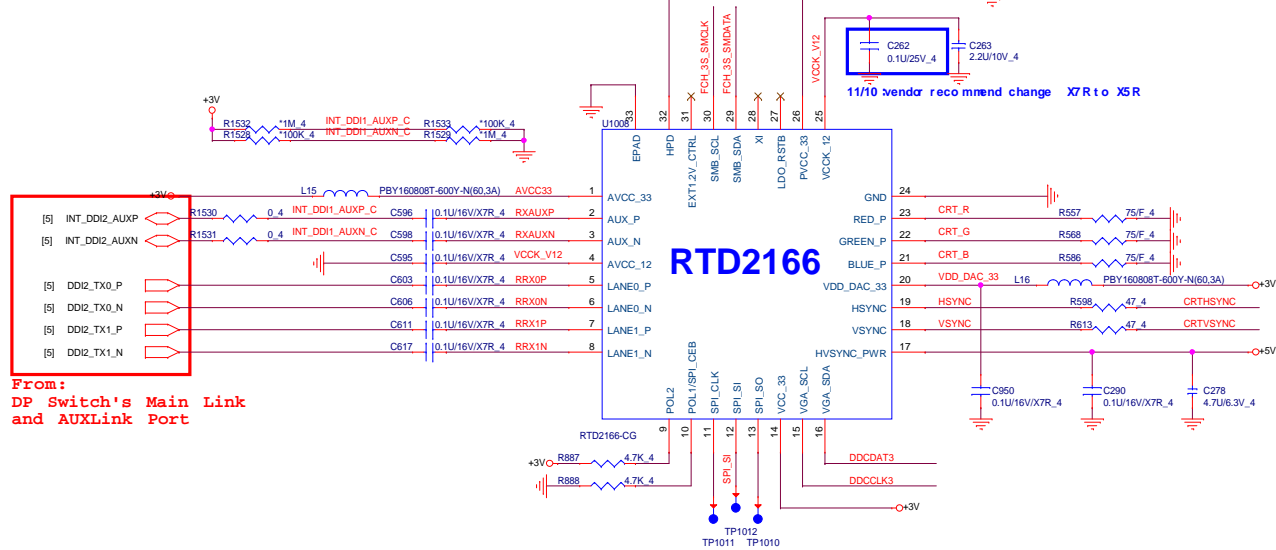
26



GS12401-1011-9H
51519-0400t-v02-40p-l



To:
DP Switch's HPD Input Port
[5] DDI_HPD_CON
Pull down at SOC side



Need check footprint and PN DFDS15FR456 dsb-10556-15002-15p

FCH_3S_SMCLK, FCH_3S_SMDATA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

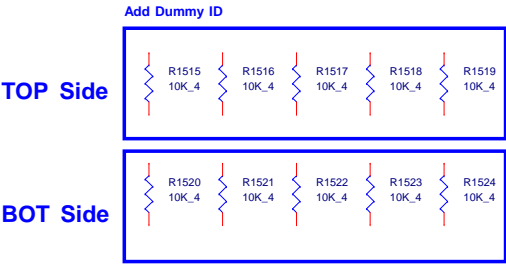
From PCH




PROJECT : X63
Quanta Computer Inc.

Size Custom	Document Number 27 - DP2VGA_converter	Rev 1A
Date: Thursday, May 19, 2016	Sheet 27 of 67	

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V _{DD}	2 dB
short to V _{DD}	short to GND	4 dB
short to V _{DD}	short to V _{DD}	6 dB



OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



PROJECT : X63

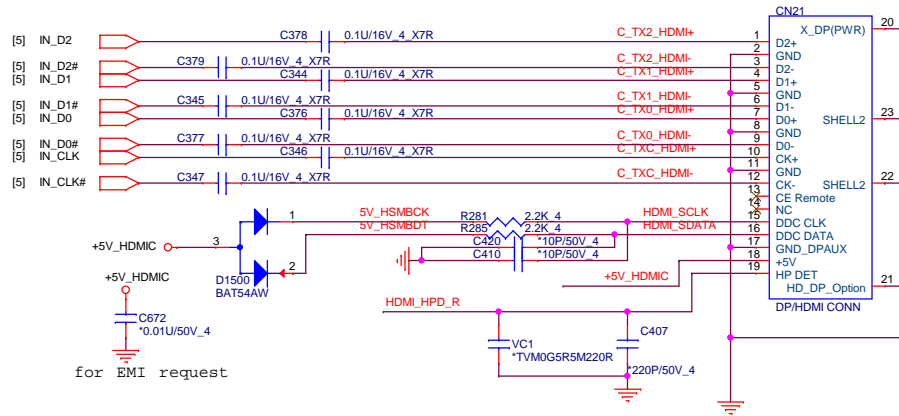
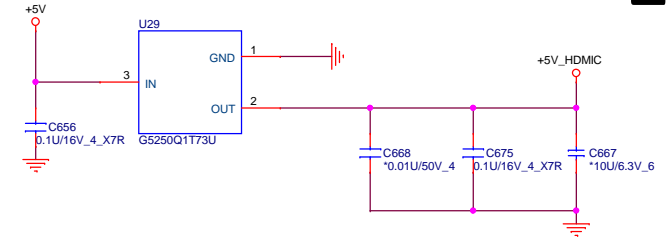
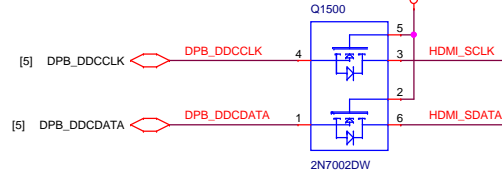
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
28 – REPEATER PTN3366		
Date: Thursday, May 19, 2016	Sheet 28 of 67	

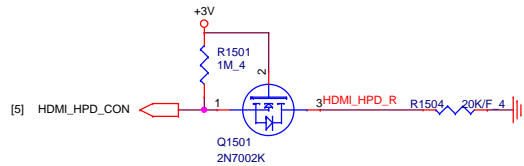
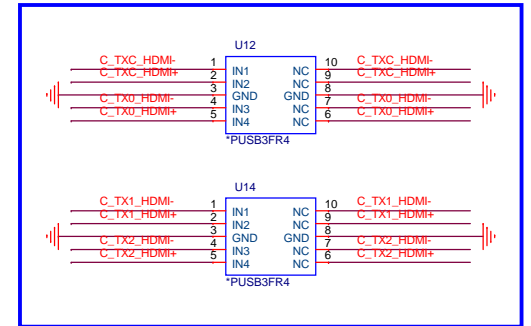
EMI Solut i on

C_TX2_HDMI+	R304	150/F 4	C_TX2_HDMI-
C_TX1_HDMI+	R291	150/F 4	C_TX1_HDMI-
C_TX0_HDMI+	R295	150/F 4	C_TX0_HDMI-
C_TXC_HDMI+	R299	150/F 4	C_TXC_HDMI-

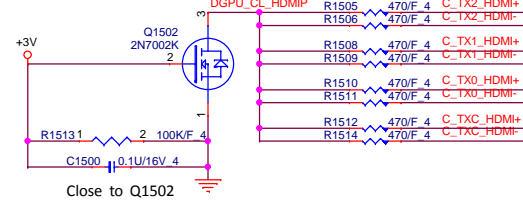
HDMI SMBus Isol at i on



for EMI request

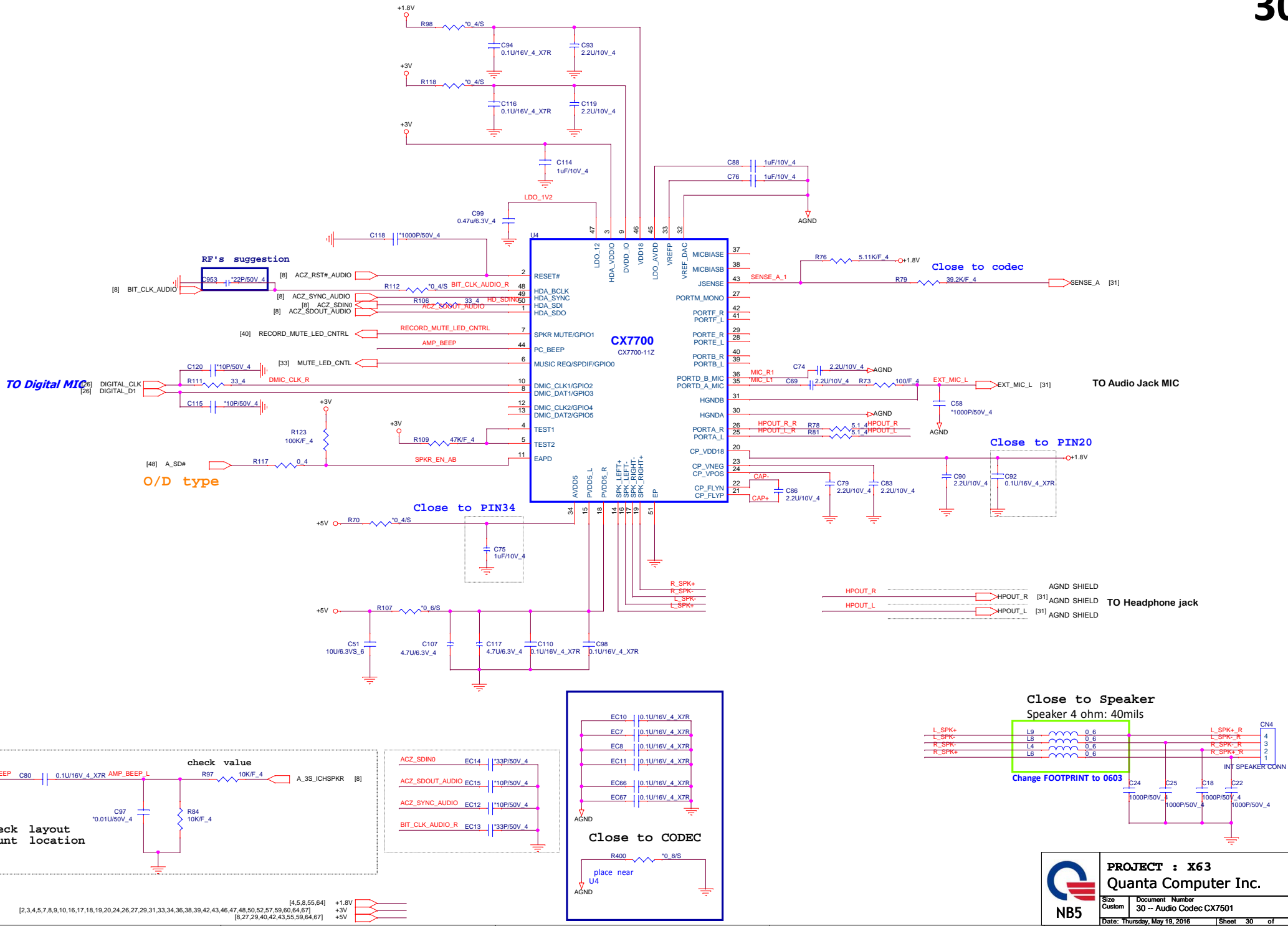


Close to HDMI connector

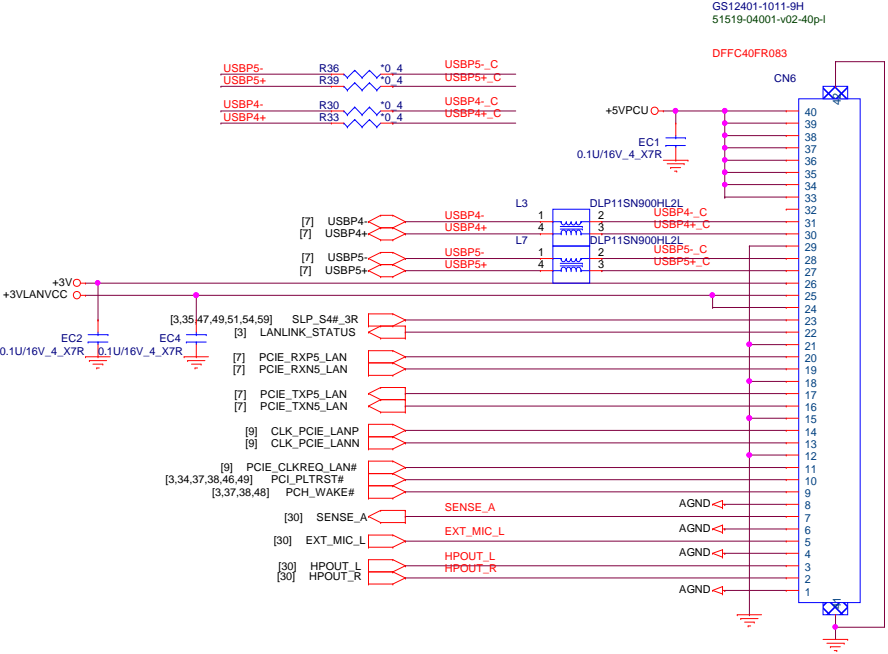


PROJECT : X63
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
29 -- HDMI CONNECTOR		
Date: Thursday, May 19, 2016	Sheet 29 of 67	

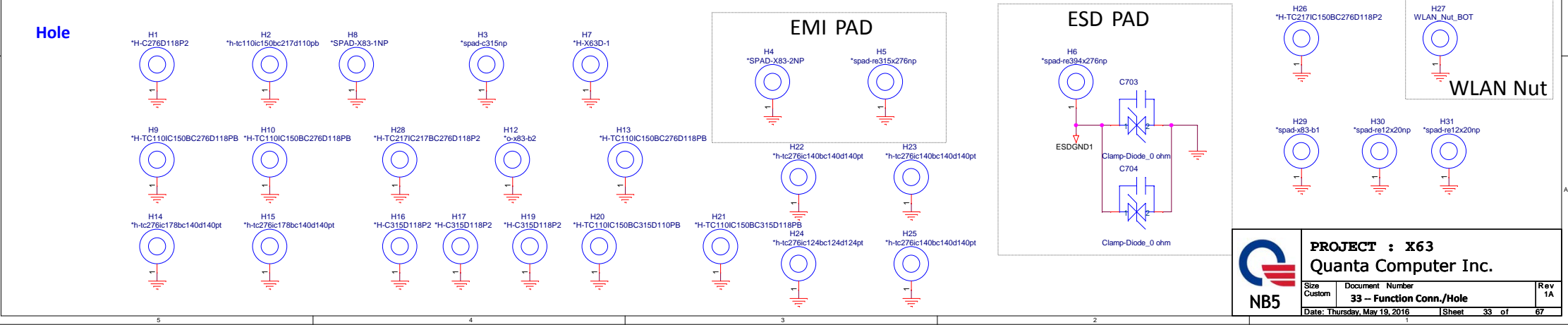
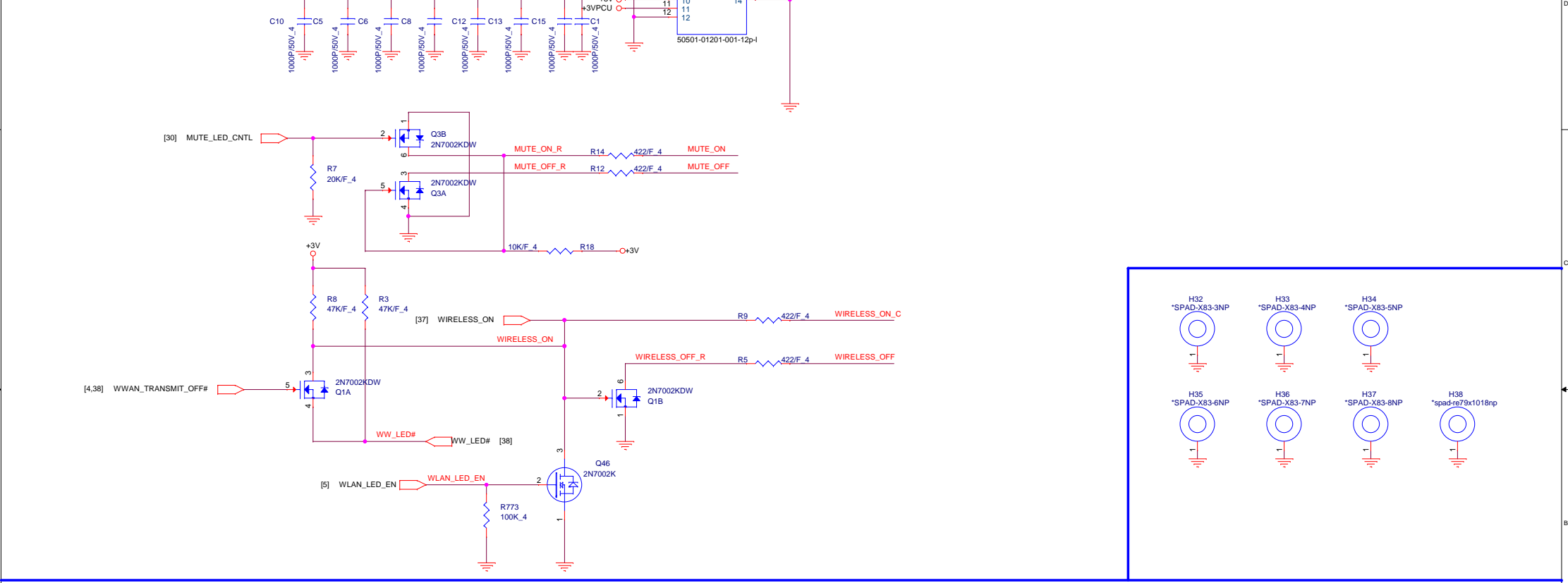


USB2.0 x2/LAN/Headphone_Mic Combo Jack Daugther Board Connector



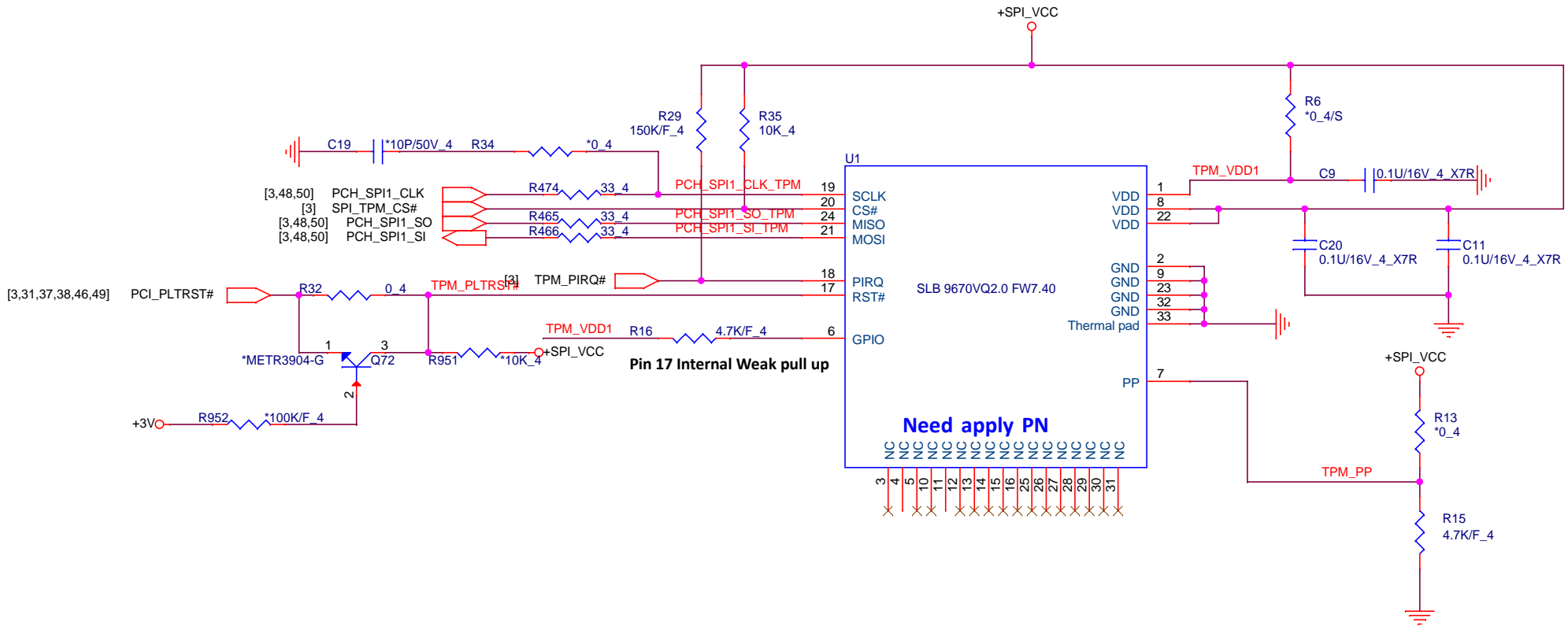
PROJECT : X63
Quanta Computer Inc.

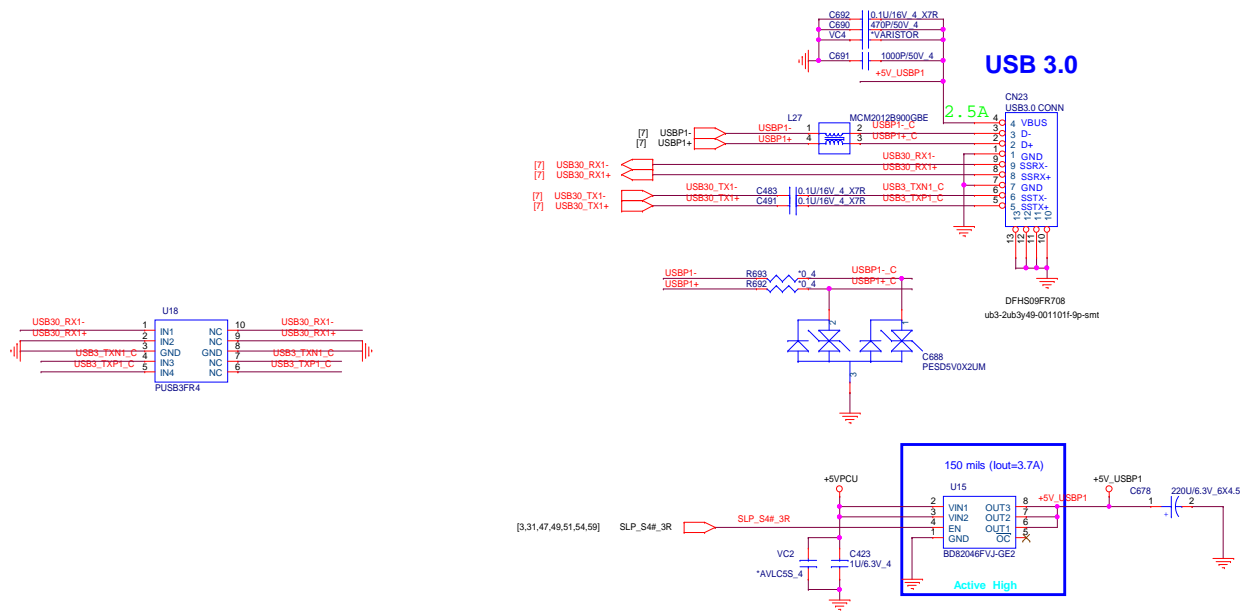
Size	Document	Number	Rev
Custom	31 -- DAUGHTER BOARD CONN.		1A
Date: Thursday, May 19, 2016 Sheet 31 of 67			



TPM (1.2 or 2.0)

34





[31,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67]
[9,41,51,52,53,59,63,64,67]

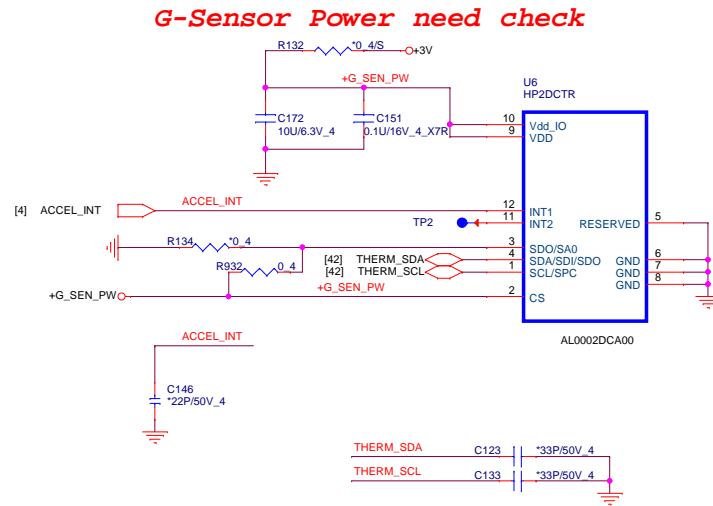
+5VPCU
+3V_ALW



PROJECT : X63
Quanta Computer Inc.

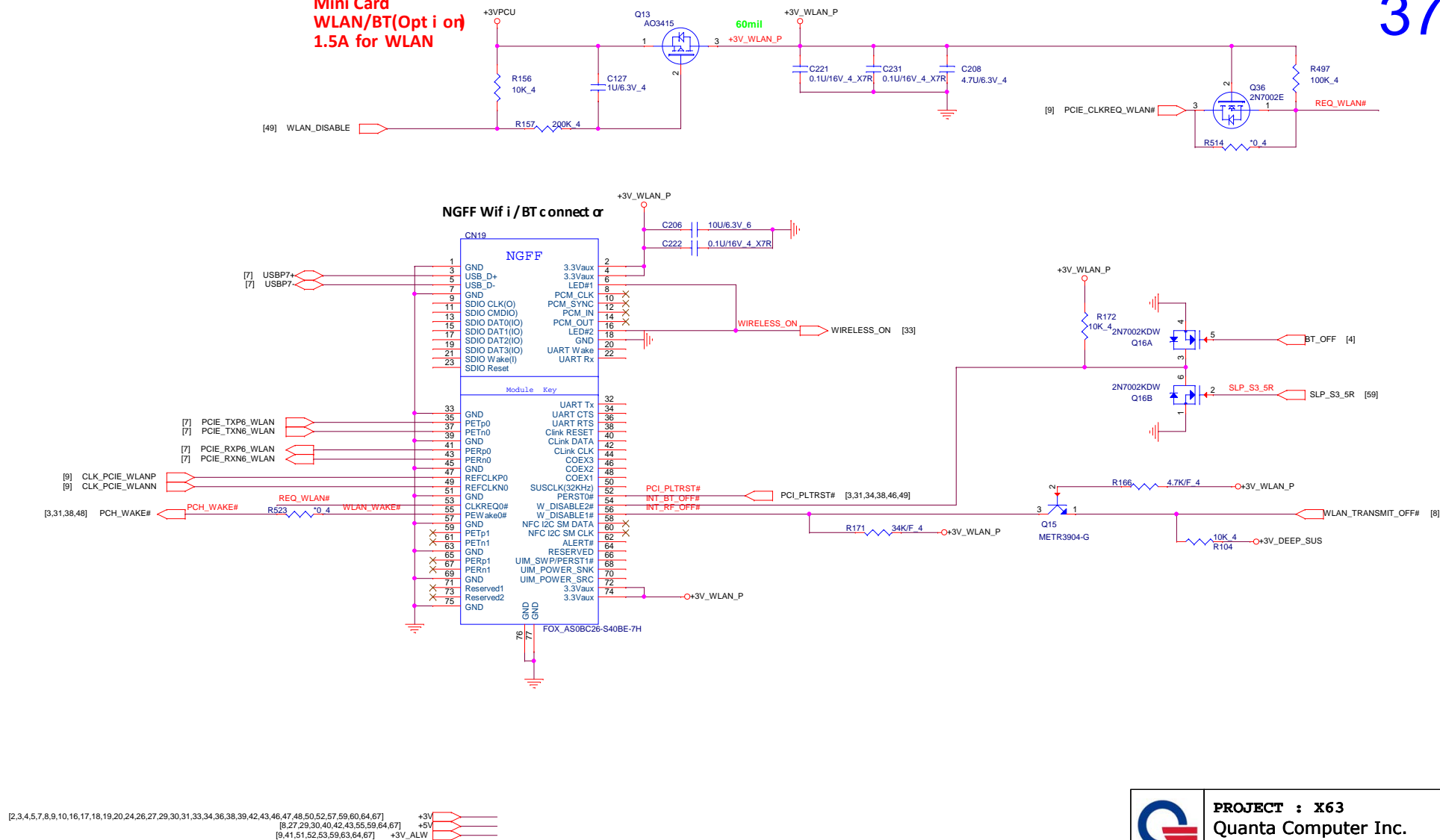
Size Custom	Document Number 35 -- USB3.0 x2	Rev 1A
Date: Thursday, Mar 19, 2016		Sheet 35 of 67

Accelerometer Sensor




[31,35,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67] +5VPCU
[9,41,51,52,53,59,63,64,67] +3V_ALW

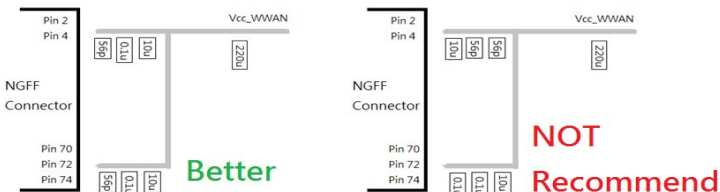
Mini Card
WLAN/BT(Optional)
1.5A for WLAN



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]
[8,27,29,30,40,42,43,55,59,64,67]
[9,41,51,52,53,59,63,64,67]

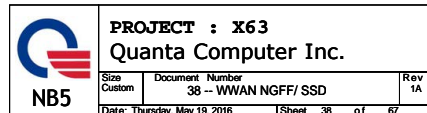
+3V
+5V
+3V_ALW

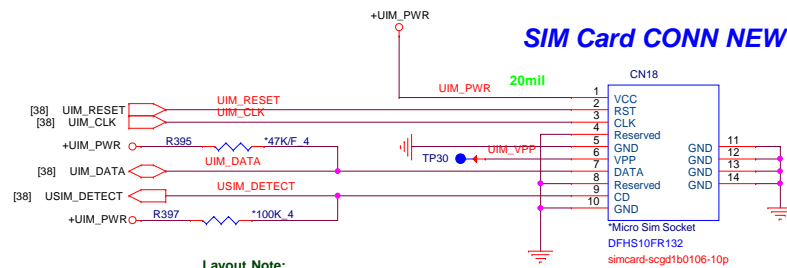
 NB5	PROJECT : X63 Quanta Computer Inc.		
	Size Custom	Document Number 37 - NGFF WLAN/BT	Rev 1A
	Date: Thursday, May 19, 2016	Sheet	37 of 67



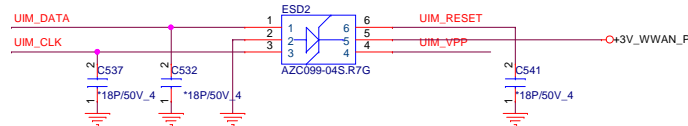
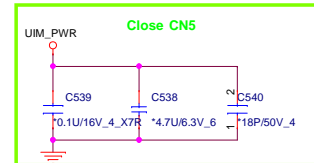
↰	M.2 Pinout ↰	S0↰	S3 – S5↰
WWAN 3.3V↰	2, 4, 70, 72, 74↰	On↰	Off↰

+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	SPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low



**Layout Note:**

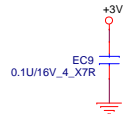
1. UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible
Route into ESD then go out
2. Avoid routing the SIM_CLK and SIM_DATA lines in parallel over distances ≥ 2 cm
3. Position the SIM connector from the WWAN module ≤ 100 mm if possible,
NOT exceed length is 150mm.

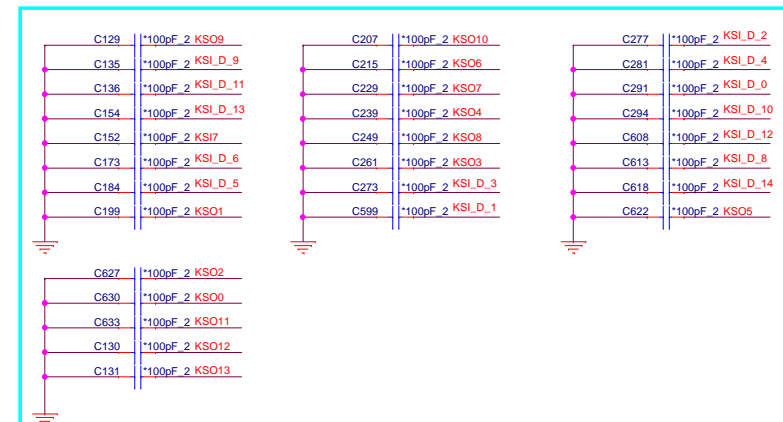
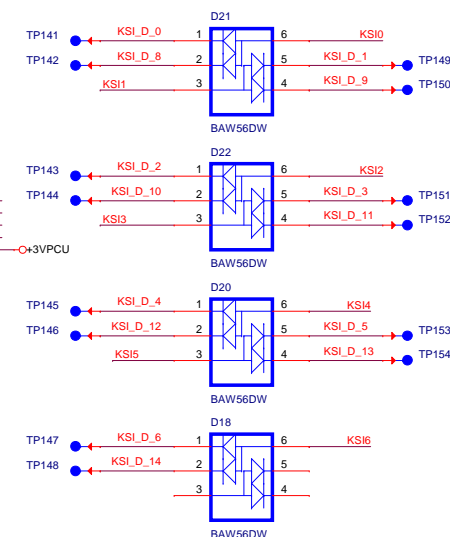
**Trace Length and Routing**

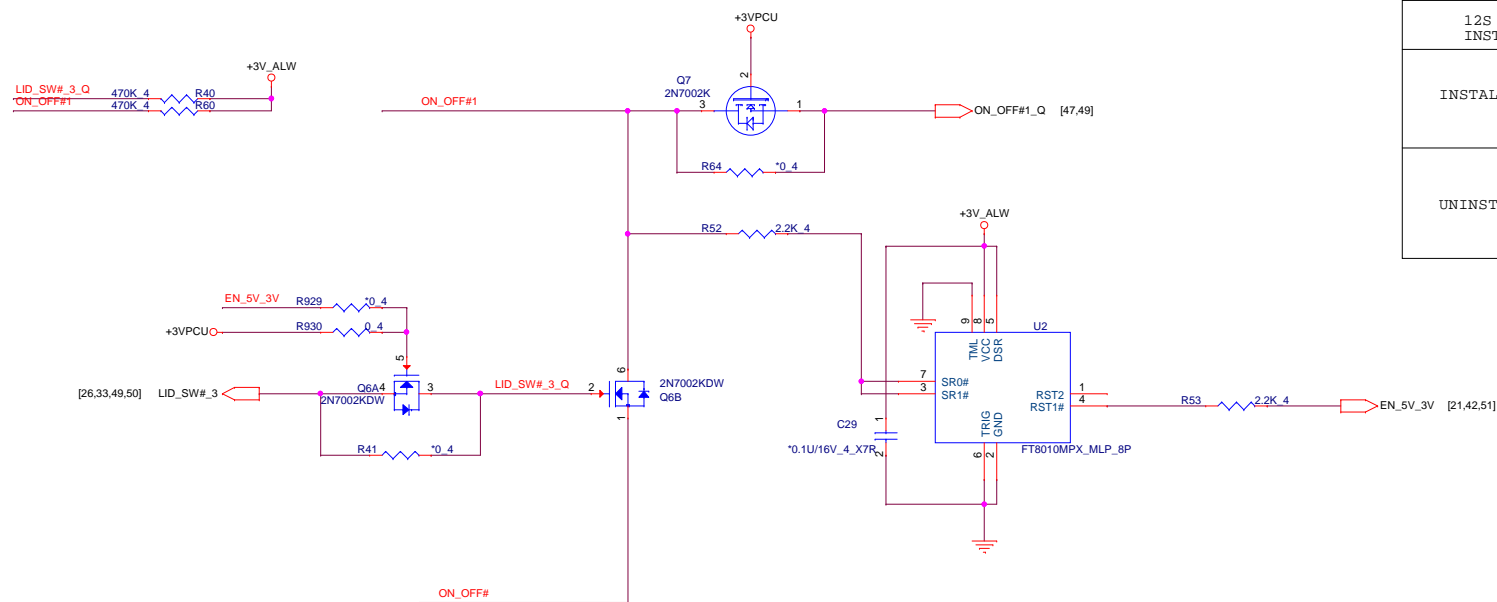
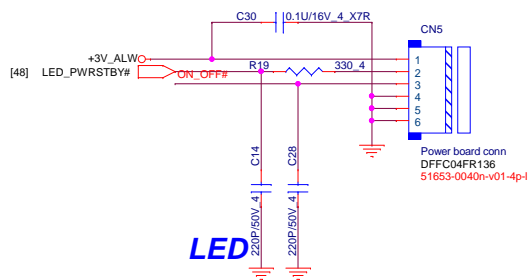
- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

SIM Power

- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.



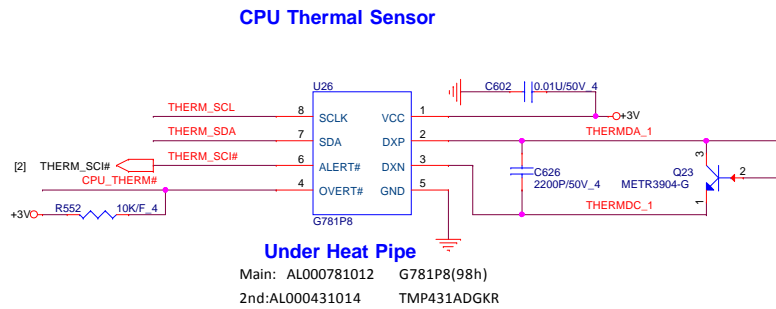




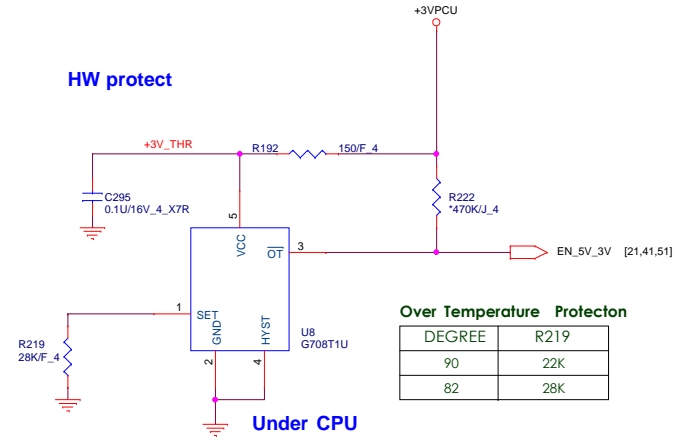
12S RESET MODE INSTAL FOR DB0		
INSTAL	R10702 R10704 R10701 U9068	R1070 R? R?
UNINSTAL	R? Q7080	R? Q7081



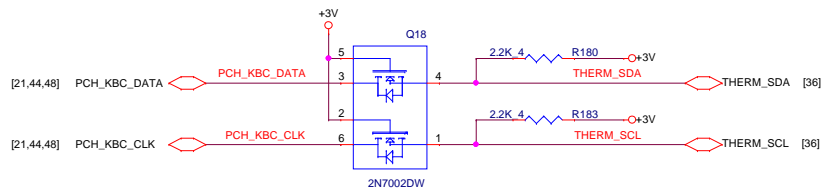
Thermal sensor



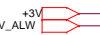
HW protect



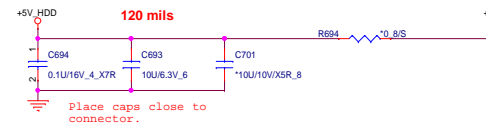
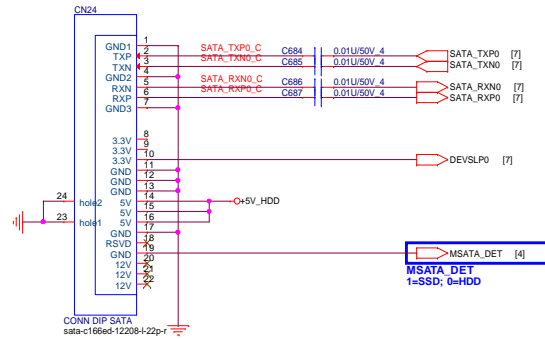
$$R_{SET} \text{ (K OHM)} = 0.0012T^2 - 0.9308T + 96.147$$



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,43,46,47,48,50,52,57,59,60,64,67]
[9,41,51,52,53,59,63,64,67]

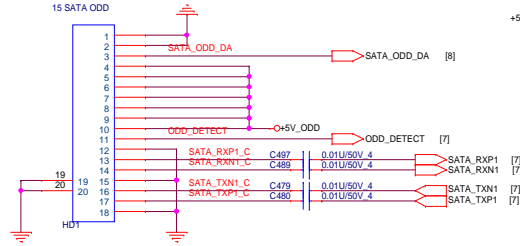


SATA-HDD



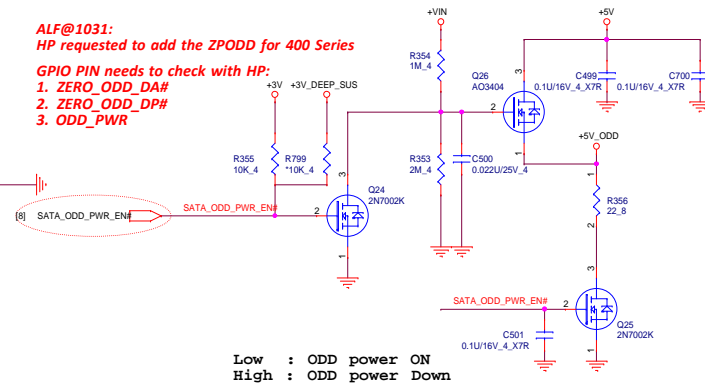
SATA-ODD

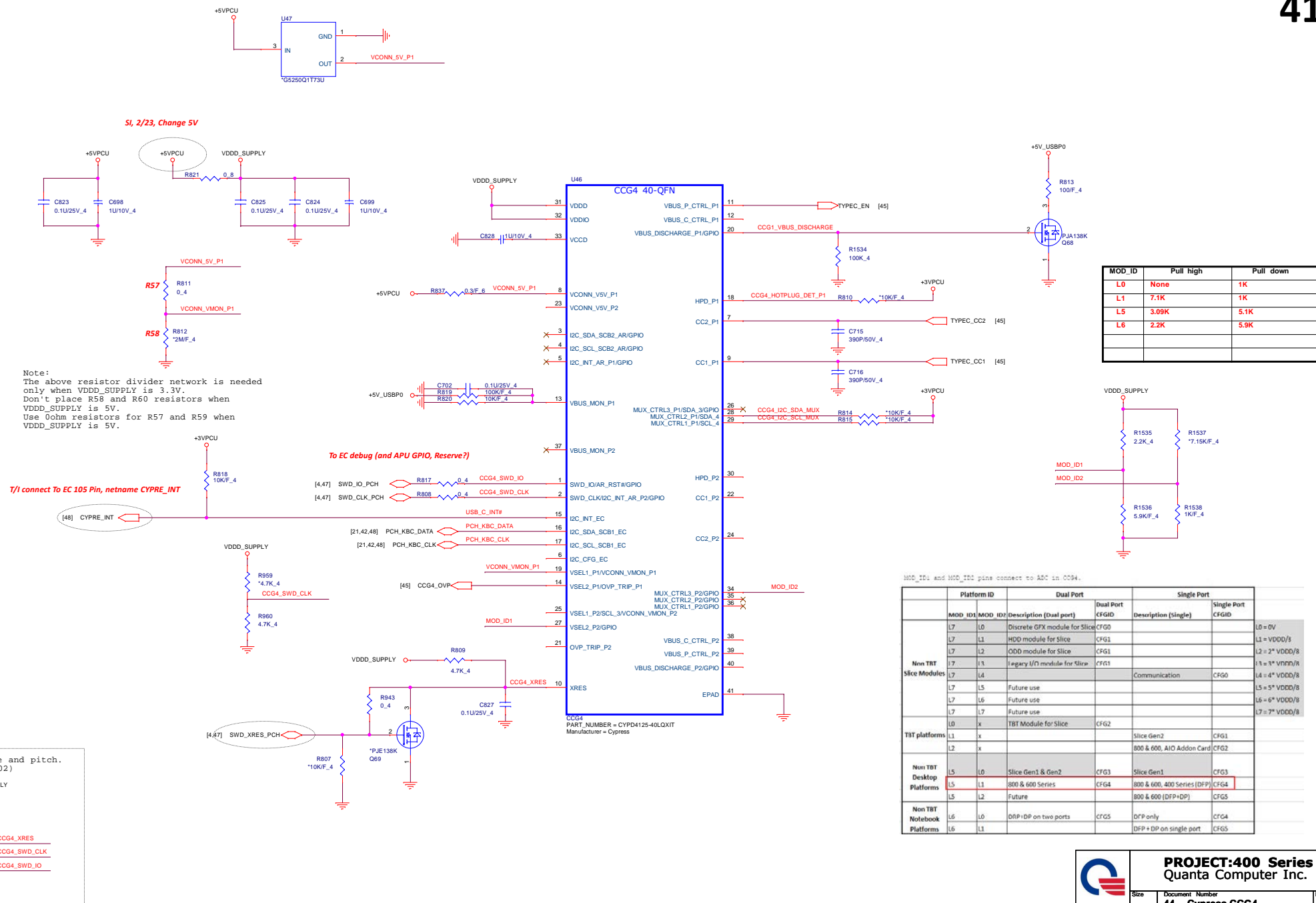
1028@Ronny: change to Vine 15" CONN



ALF@1031:
Close to Conn Pin

ALF@1031:
HP requested to add the ZPODD for 400 Series
GPIO PIN needs to check with HP:
1. ZERO_ODD_DA#
2. ZERO_ODD_DP#
3. ODD_PWR





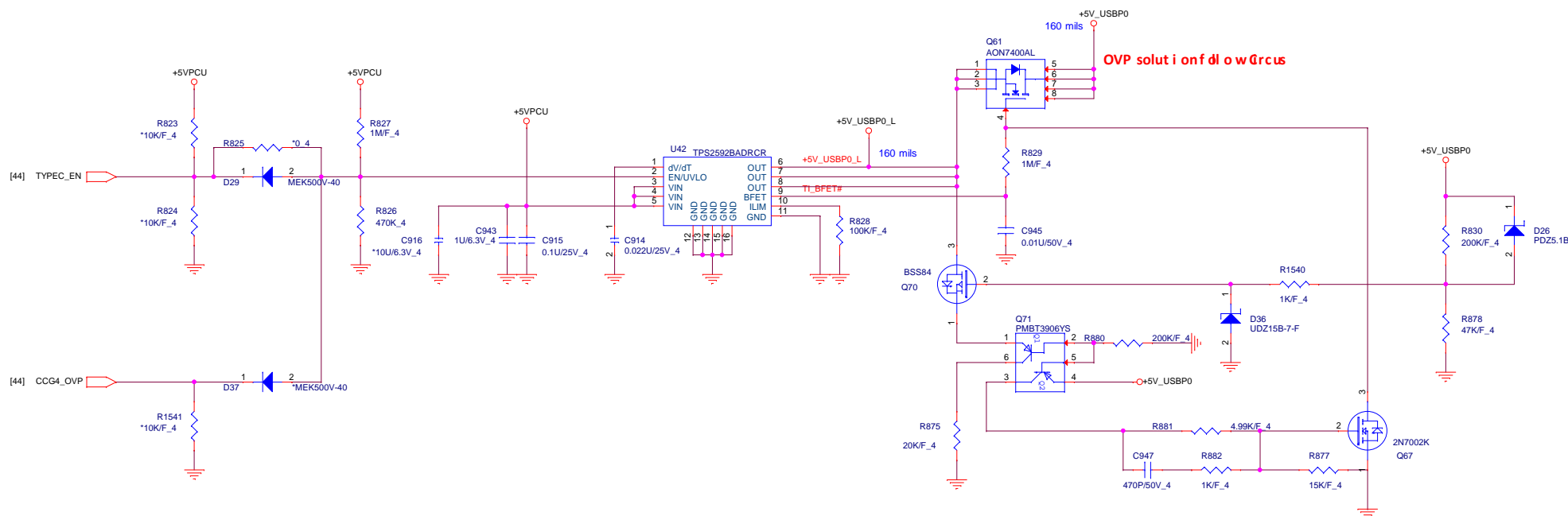
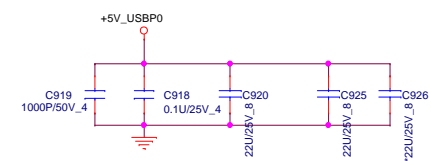
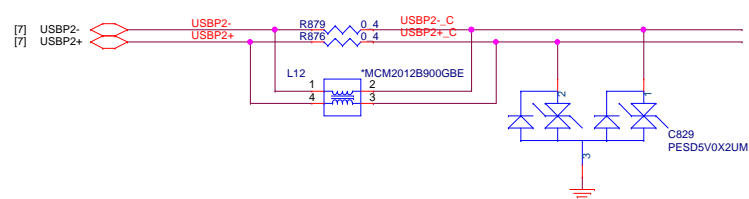
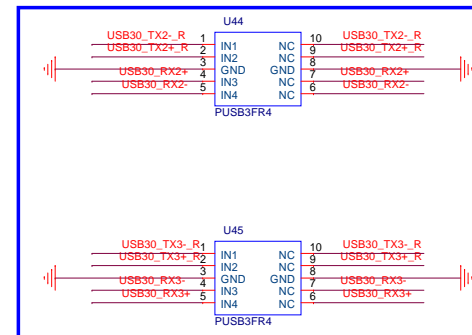
PROJECT:400 Series
Quanta Computer Inc.

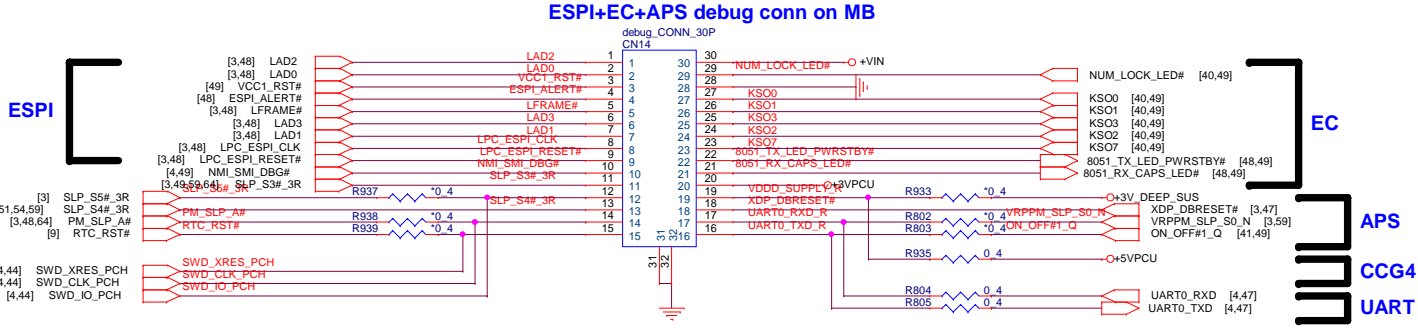
Size Document Number
44 - Cypress CCG4

Date: Thursday, May 19, 2016 Sheet 44 of 67

NB5

Rev 1A





LPC_ESPI_CLK *0.4 R369 *10P/50V 4 C508

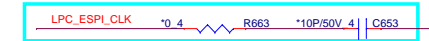
47] UART0_RXD R364 49.9K/F 4

47] UART0_TXD R365 49.9K/F 4

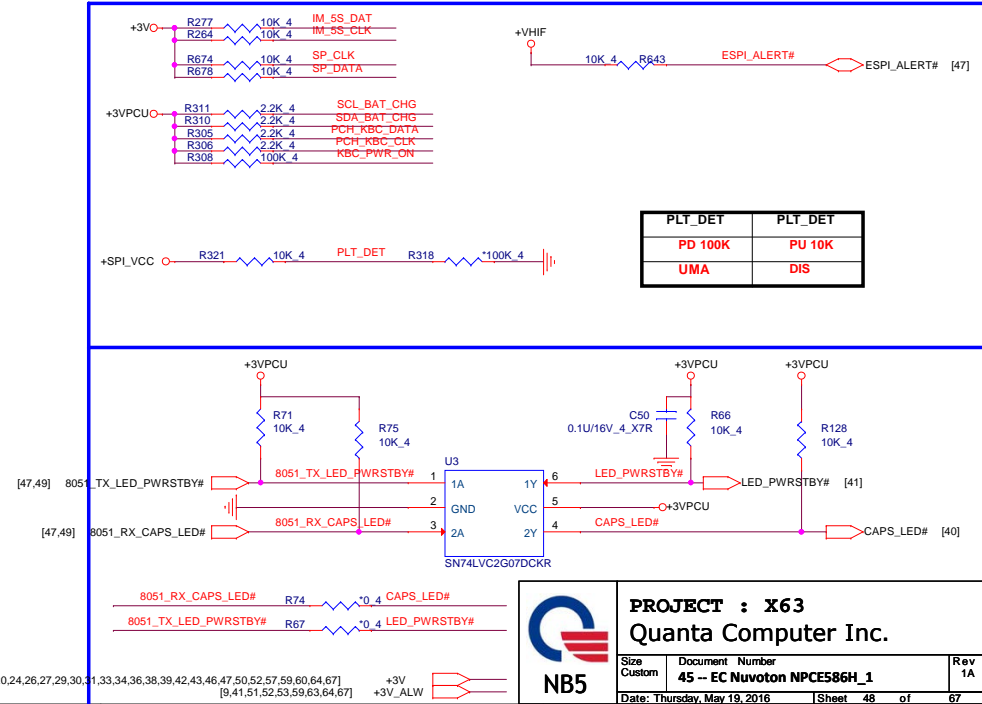
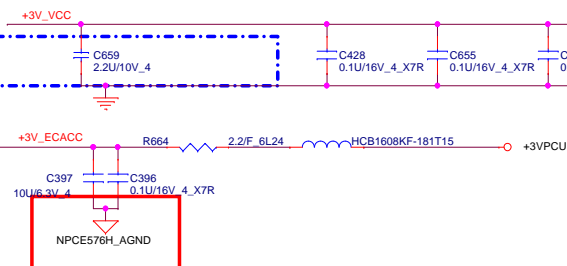
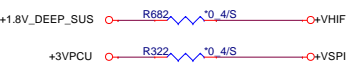
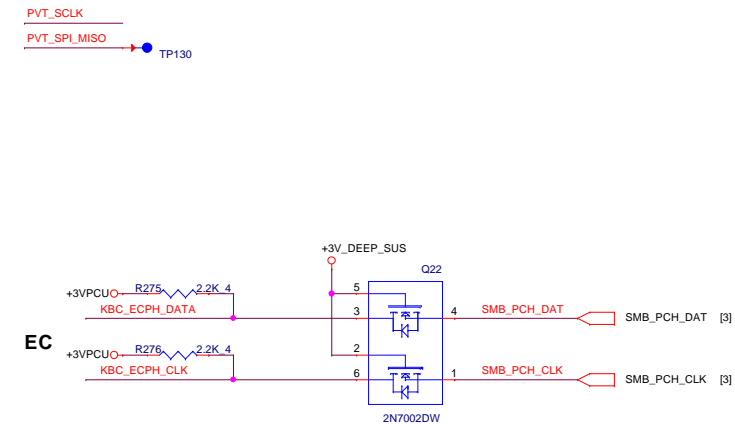
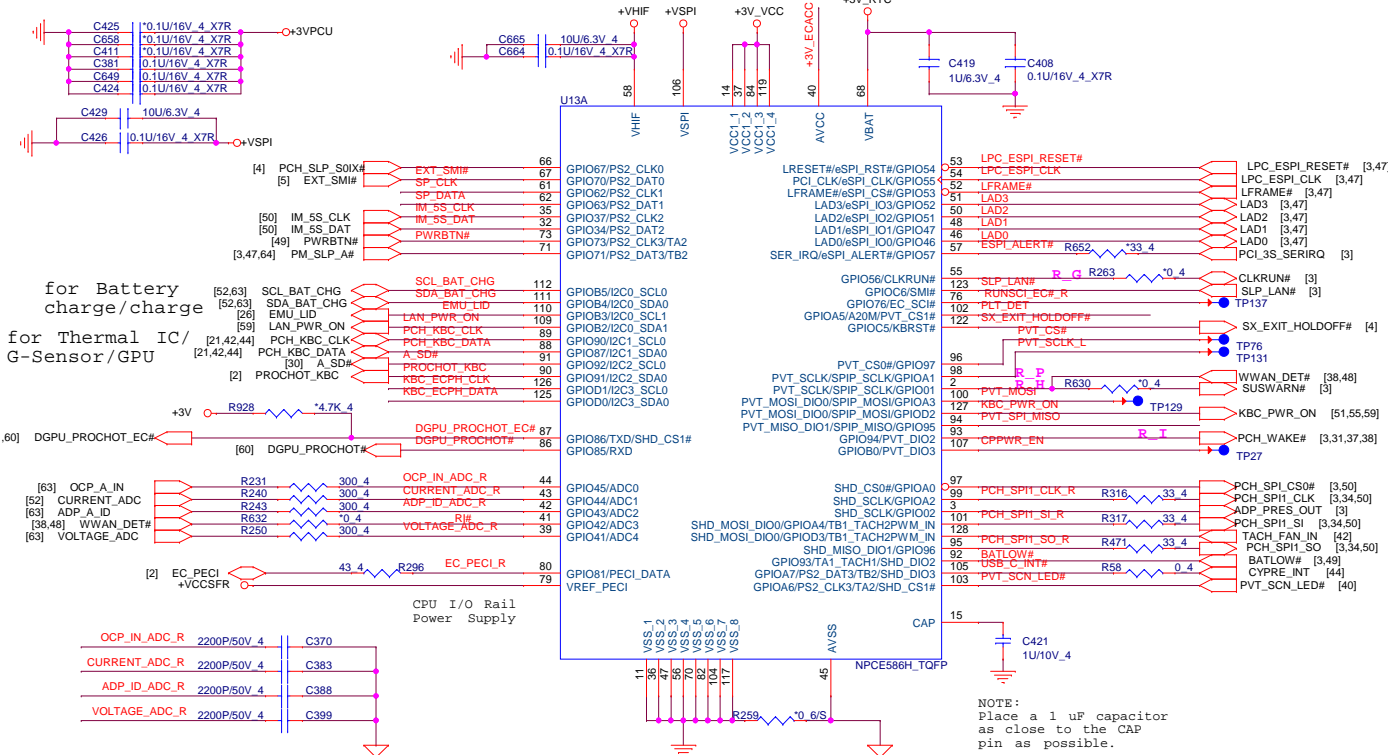
+3V

+3V R159 10K 4 XDP_DBRESET# XDP_DBRESET# [3,47]

For EMI reserved



	eSPI Mode	LPC Mode
R263 R_G	Un-Install	Install
R630 R_H	Un-Install	Install
R307 R_I	Un-Install	Install
R631 R_P	Install	Un-Install



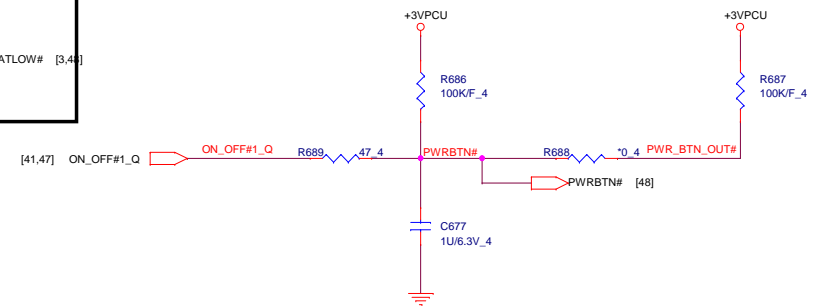
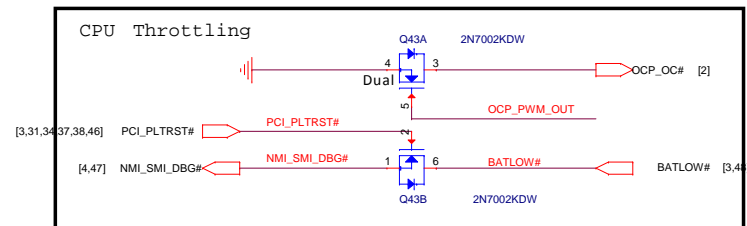
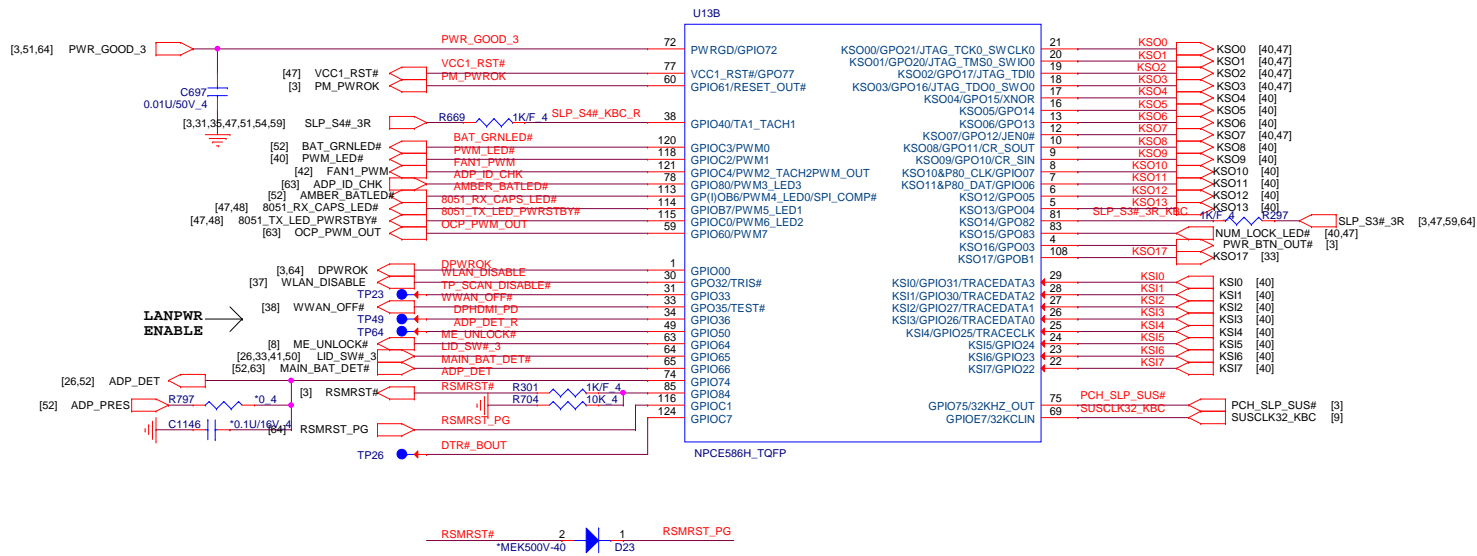
PLT_DET	PLT_DET
PD 100K	PU 10K
UMA	DIS



PROJECT : X63
Quanta Computer Inc.

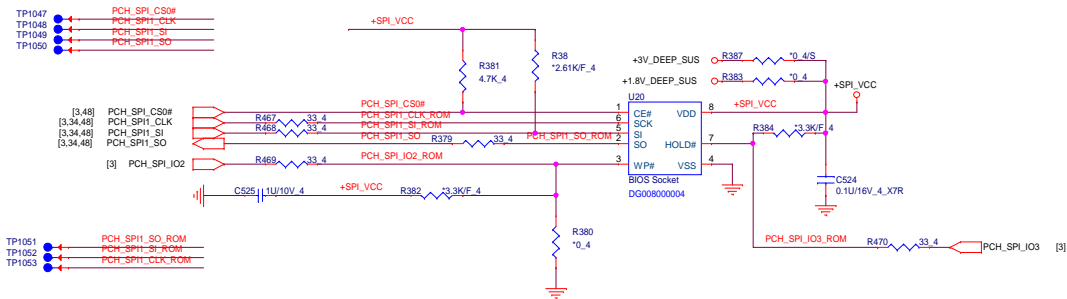
Size	Document Number	Rev
Custom	45 - EC NuvoTon NPCE586H_1	1A
Date: Thursday, May 19, 2016	Sheet 48 of 67	

[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,50,52,57,59,60,64,67]
 [9,41,51,52,53,59,63,64,67]

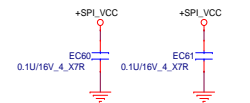


Vender	Size	P/N
Winbond	8MB	AKE3EFPKN01
Winbond	16MB	AKE3DZN0N01 SI :02' 02
Socket		DFHS08FS046

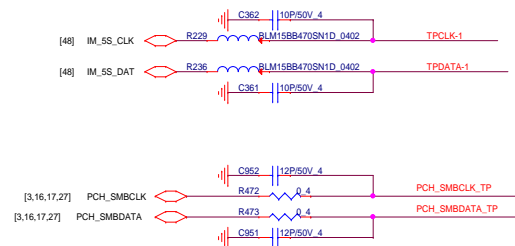
PCH SPI ROM(CLG)

PCH 6*5mm WSON 16M
SPI ROM Socket

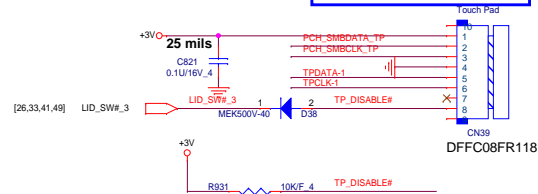
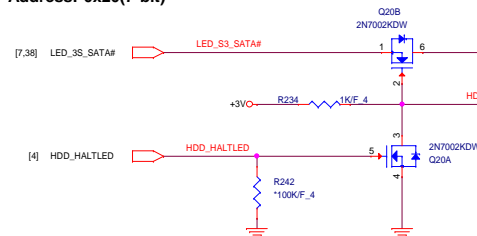
For EMI Reserved



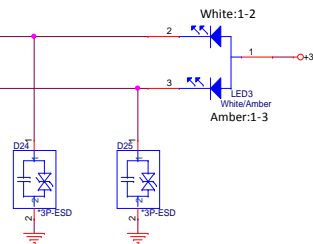
Touch pad



Forced Pad Connector

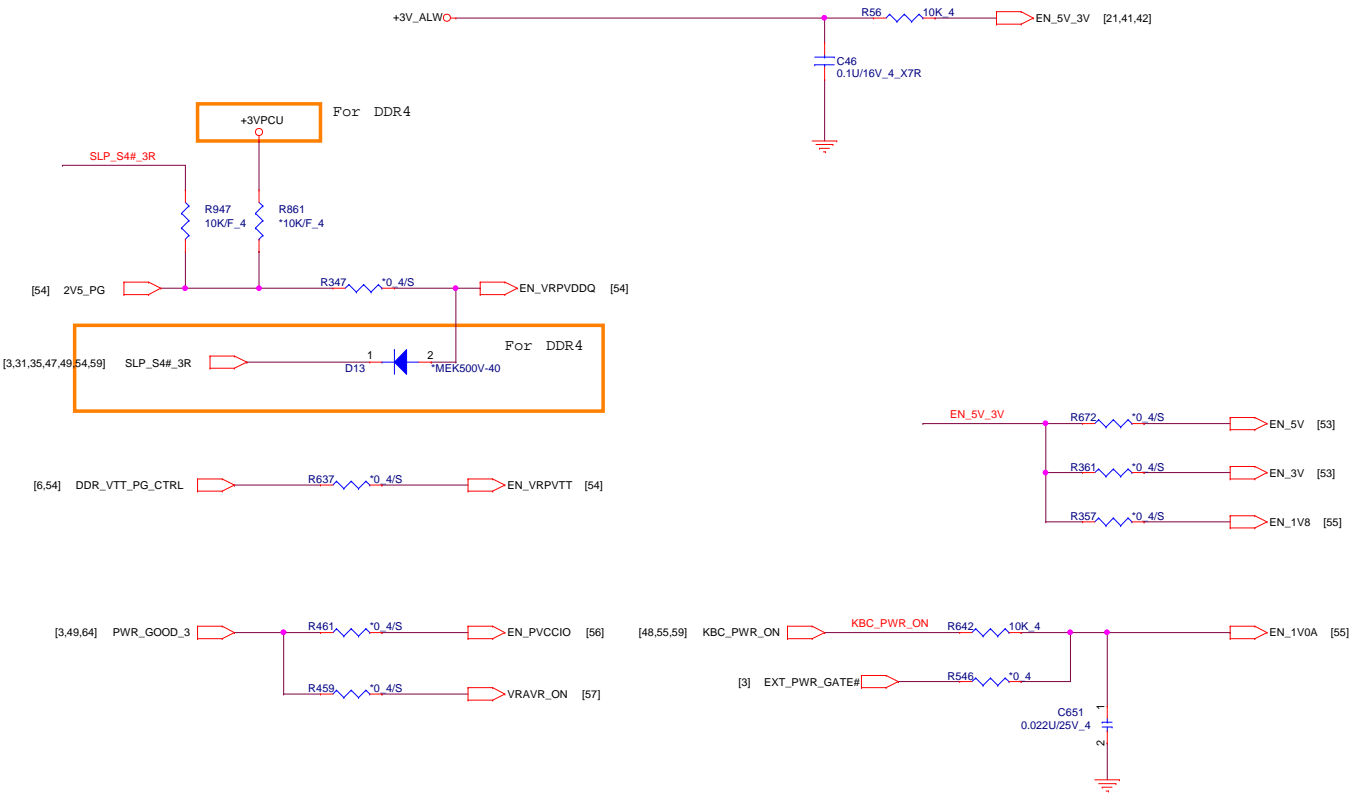
CLICK PAD
Address: 0x20(7 bit)

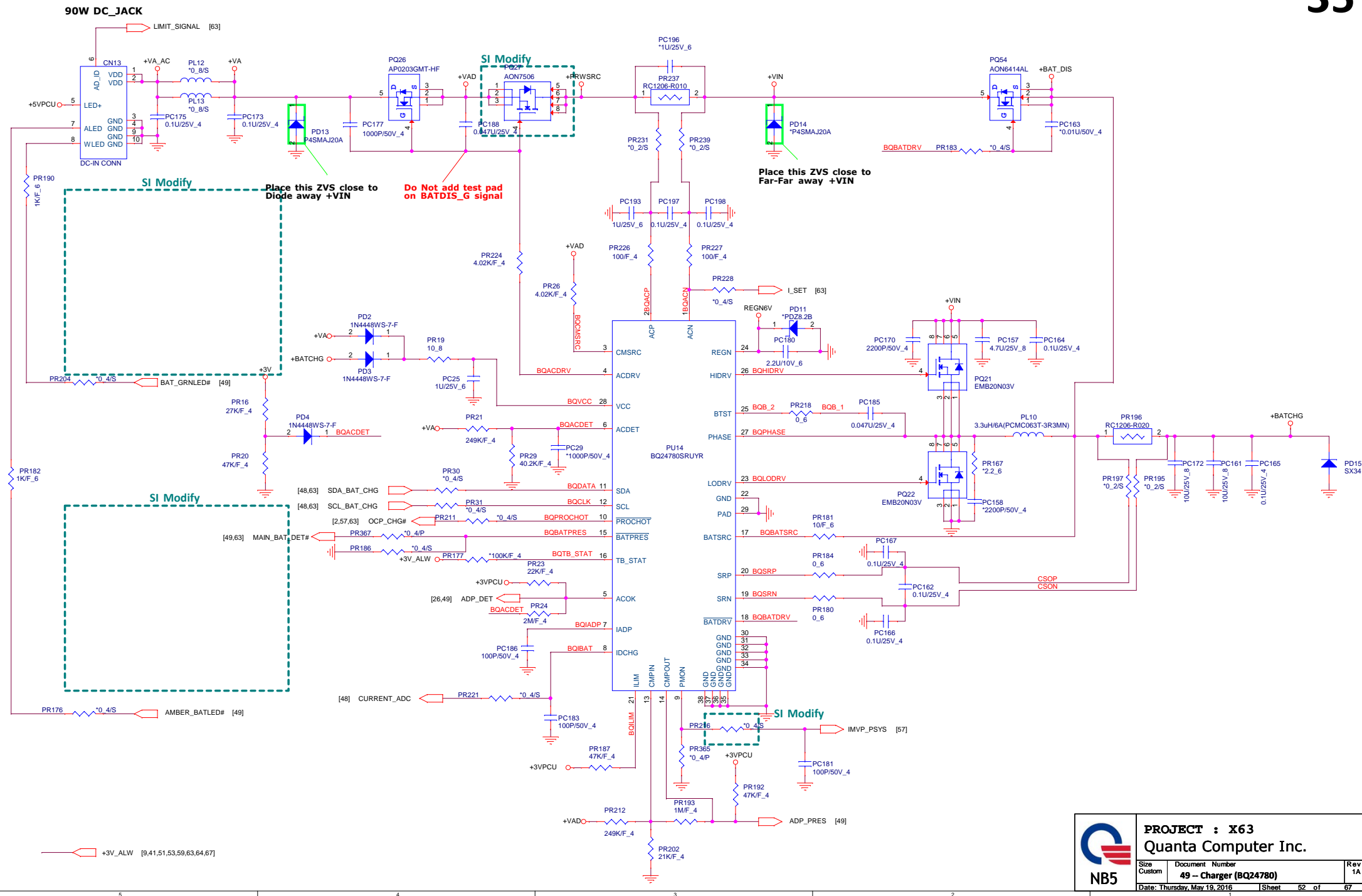
HDD LED



PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	47 - Flash(KBC+PCH)/ Touch pad	1A
Date: Thursday, Mar 19, 2016	Sheet 50 of 67	

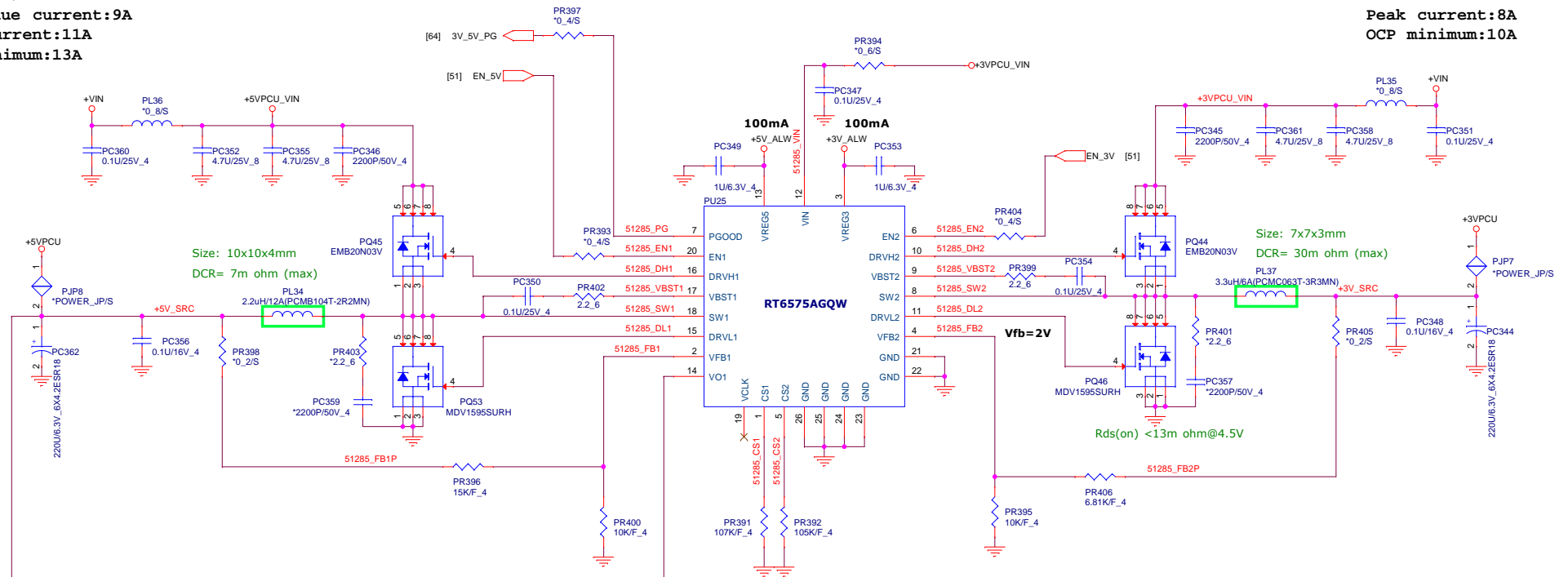


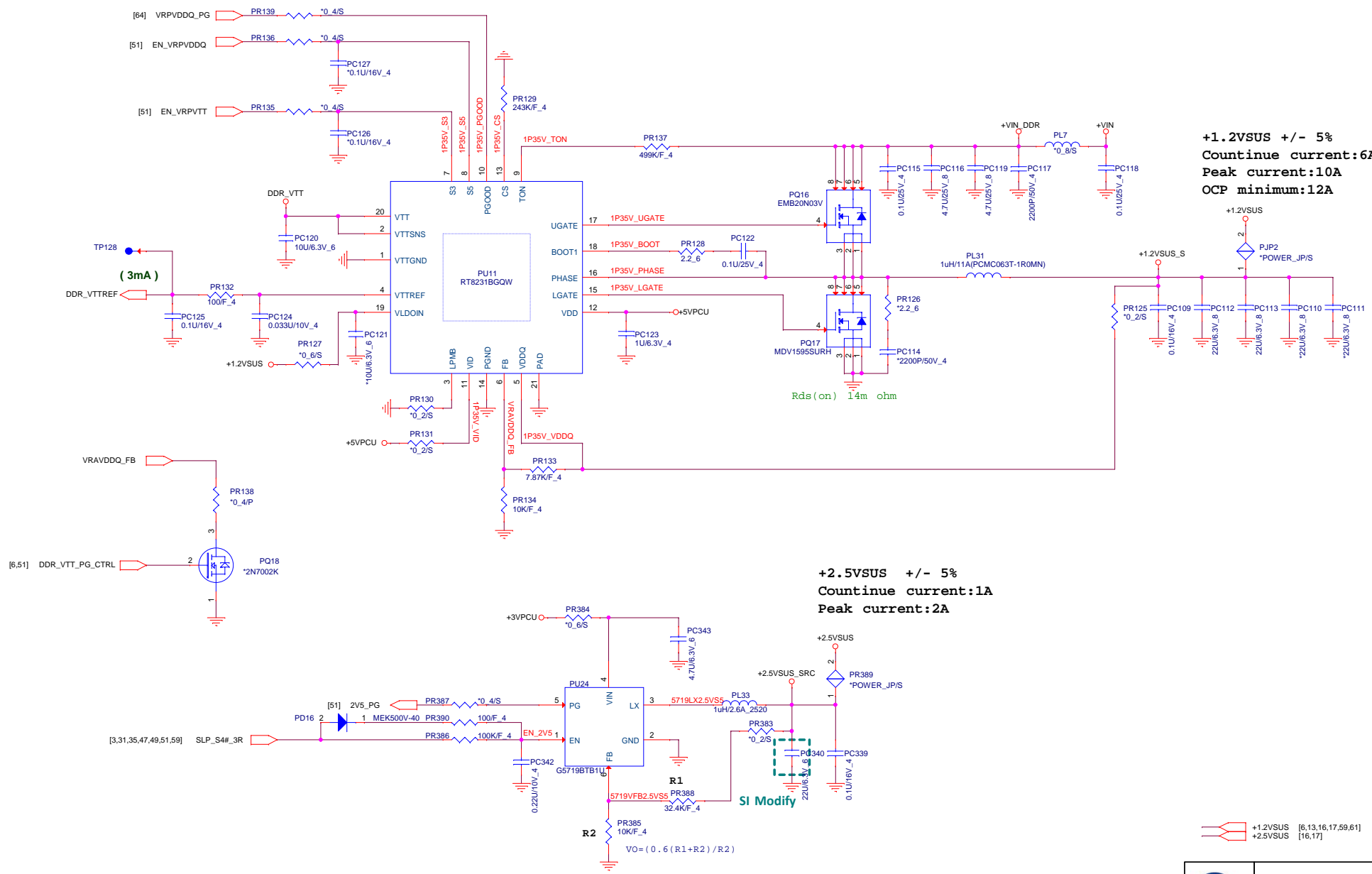


+3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,54,56,59,61,63,64,67]
 +5VPCU [31,35,44,45,46,47,52,54,55,57,58,59,60,61,62,64,67]

+5VPCU +/- 5%
 Countinue current:9A
 Peak current:11A
 OCP minimum:13A

+3VPCU +/- 5%
 Countinue current:6A
 Peak current:8A
 OCP minimum:10A



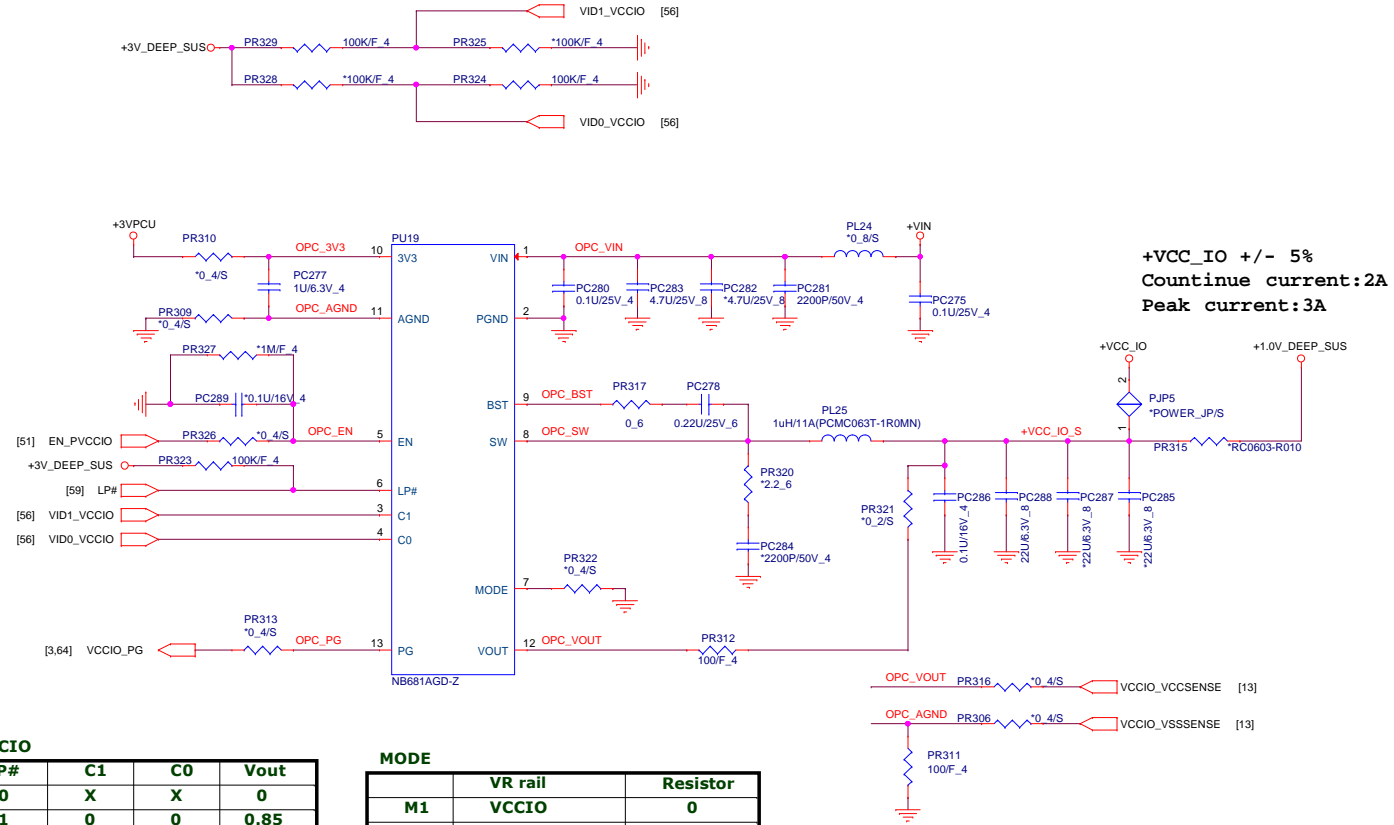


+1.2VSUS [6,13,16,17,59,61]
+2.5VSUS [16,17]



PROJECT : X63		
Quanta Computer Inc.		
Size	Document Number 1.8V ~ +1.0VS5/1.8VS5	Rev 1A
Date:	Thursday, May 19, 2016	Sheet 55 of 67

[26,43,47,52,53,54,55,57,58,59,60,62,67] +VIN
[9,41,51,52,53,59,63,64,67] +3V_ALW
[5,13] +VCC_IO

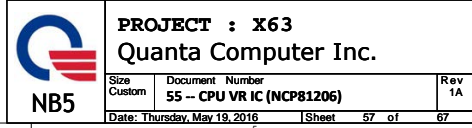


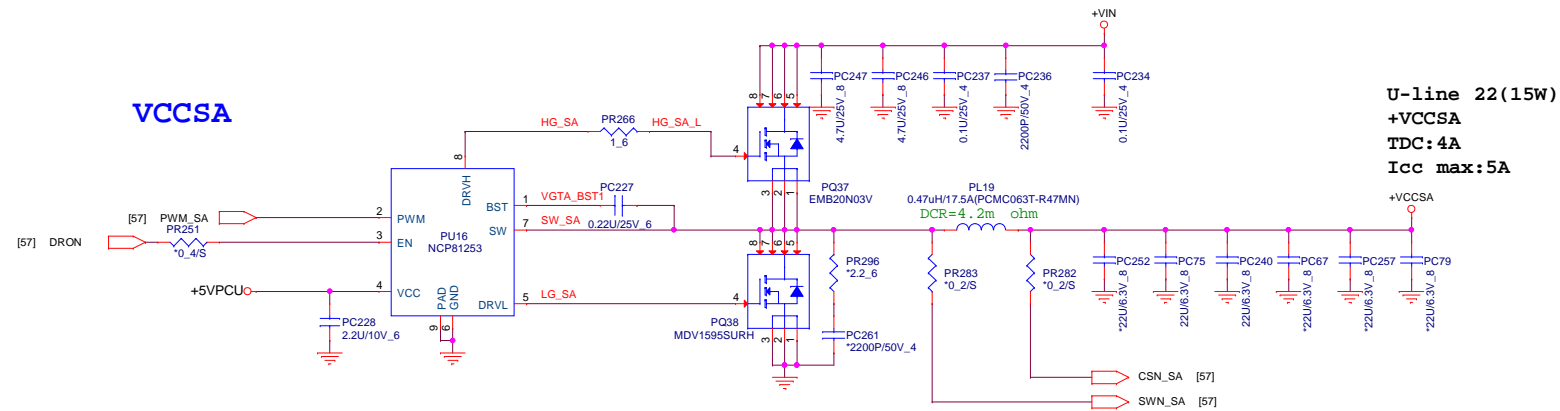
VCCIO

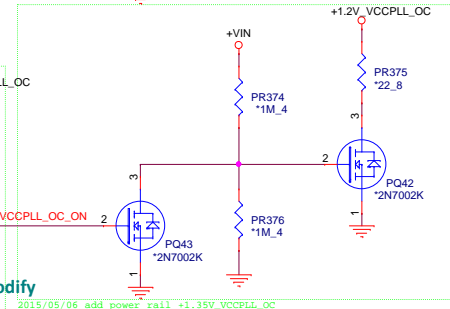
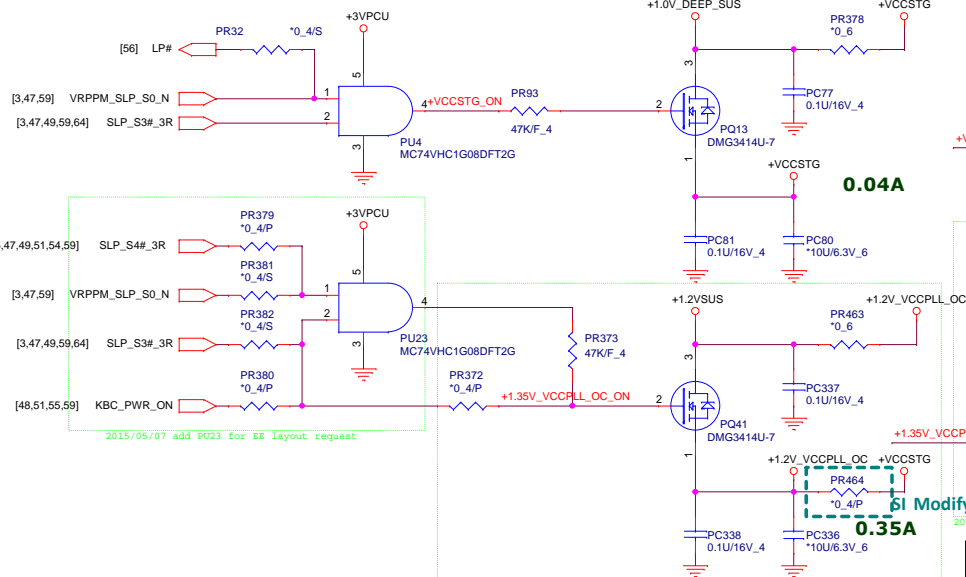
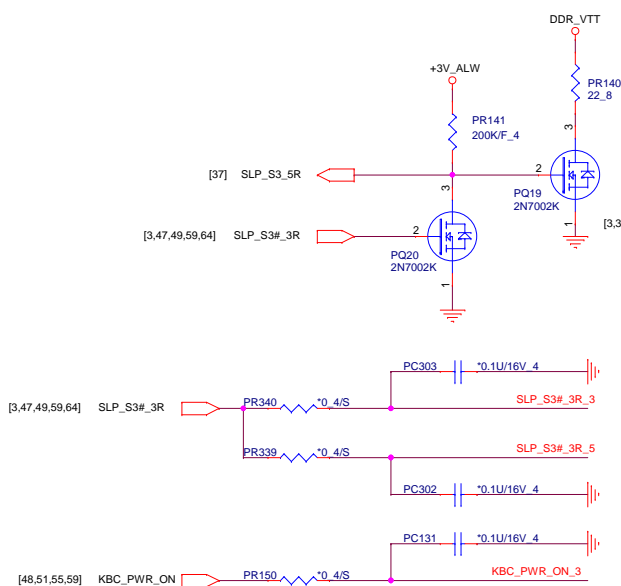
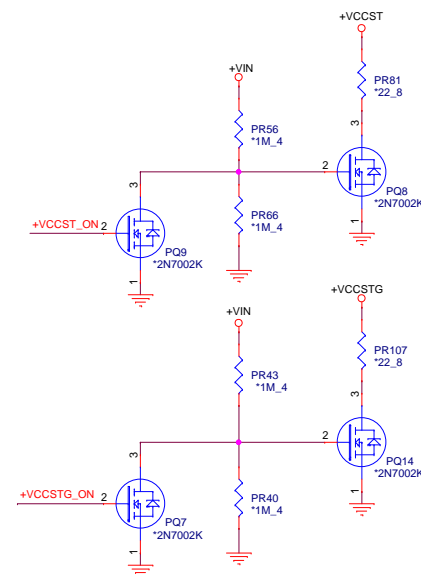
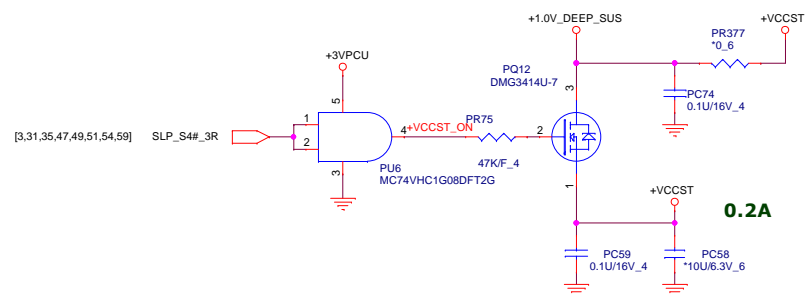
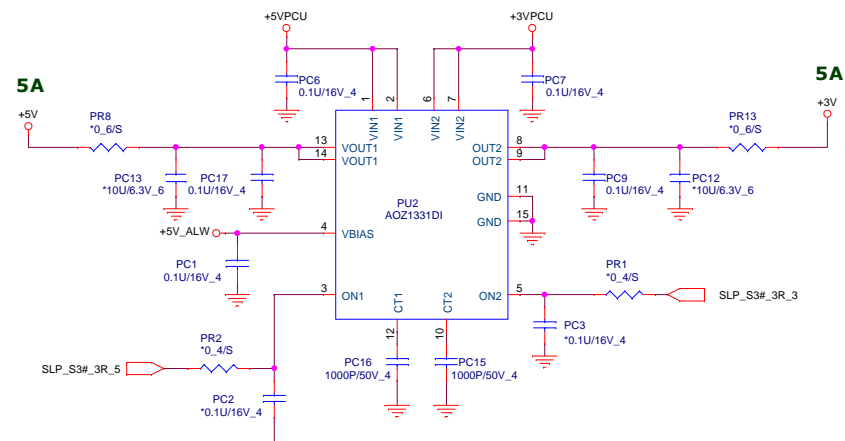
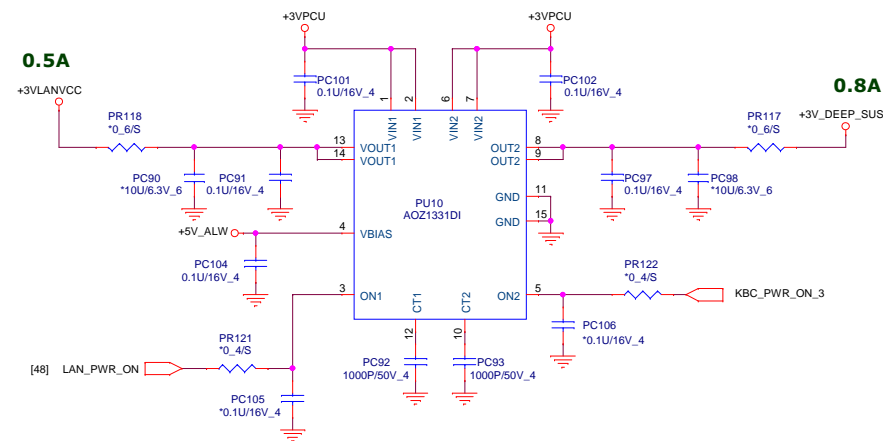
LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EPIO	100K
M4	other	150K

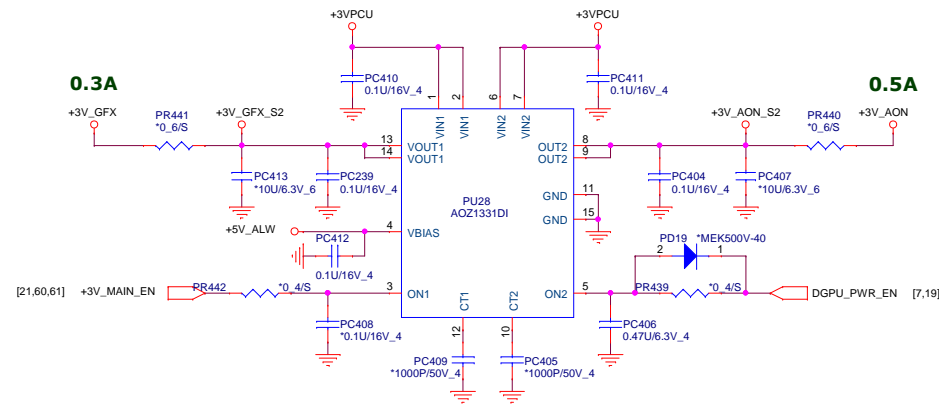
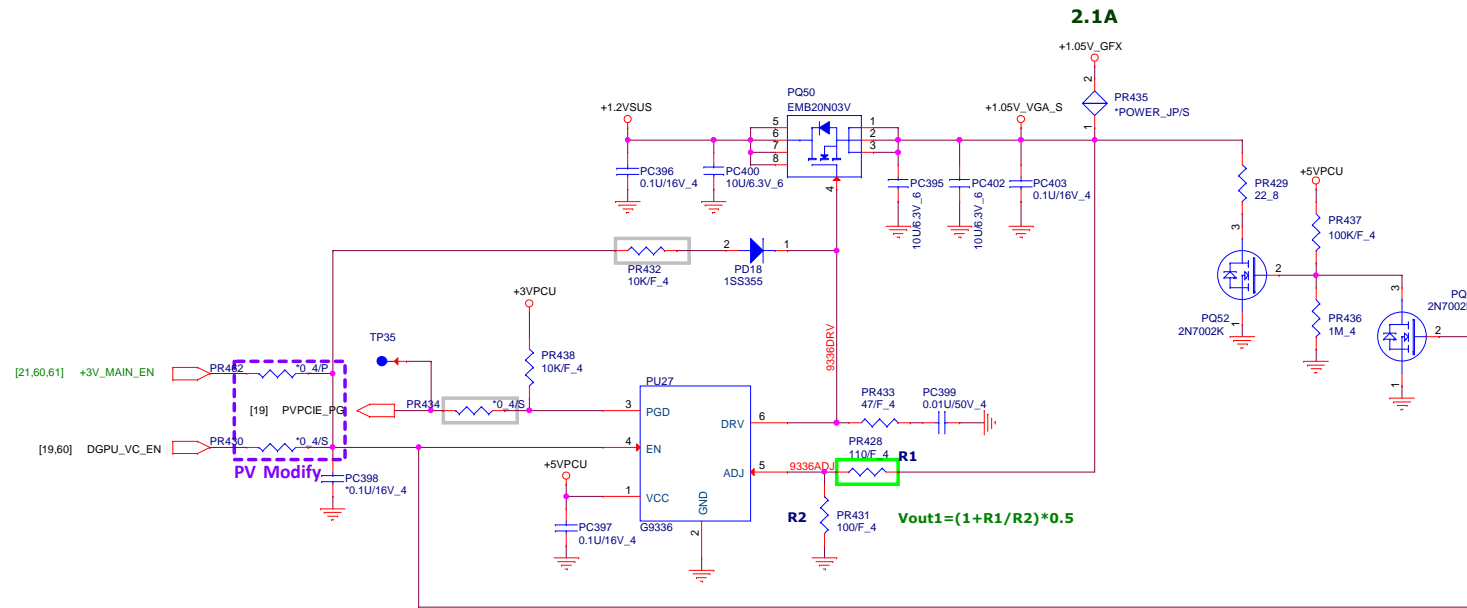






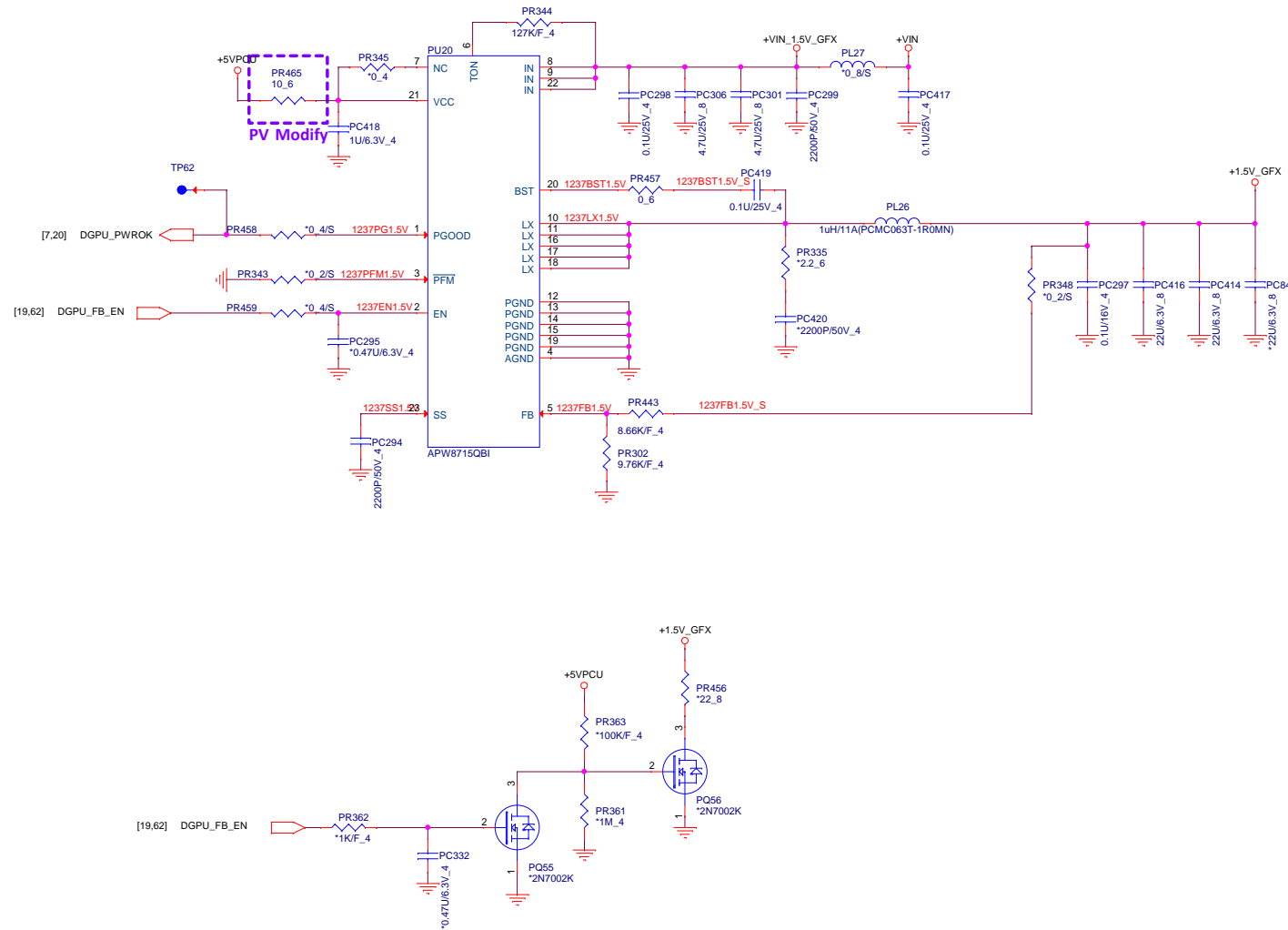
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 [8,27,29,30,40,42,43,55,64,67]
 [26,43,47,52,53,54,55,56,57,58,60,62,67]
 [3,10,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,61,63,64,67]
 [31,35,44,45,46,47,52,53,54,55,57,58,60,61,62,64,67]
 [31]

PROJECT : X63		Quanta Computer Inc.	
Size	Document Number	57 -- Load switch IC (APL3523A)	
Custom	57	Rev 1A	
Date: Thursday, May 19, 2016		Sheet	59 of 67

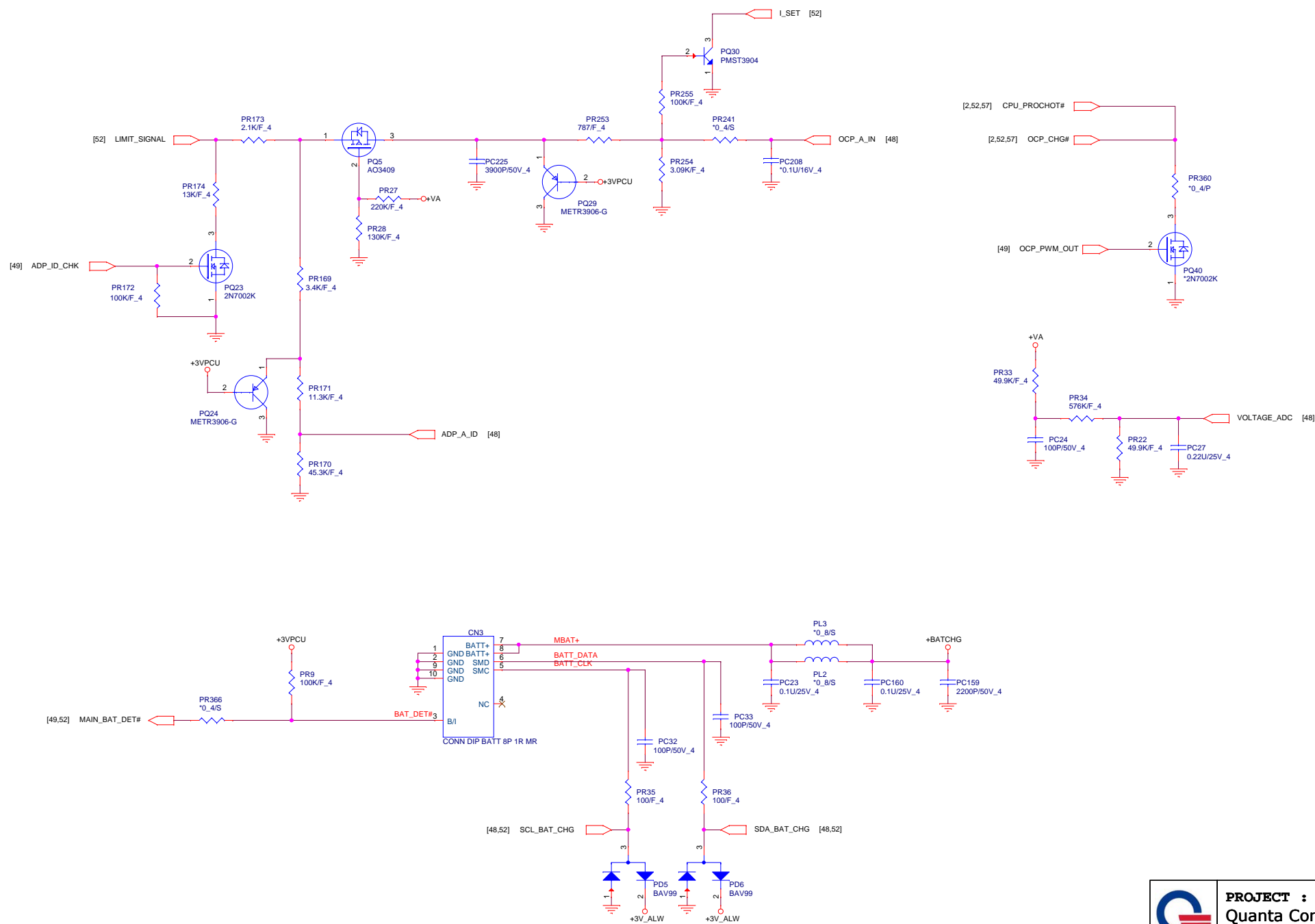


PROJECT : X63
Quanta Computer Inc.

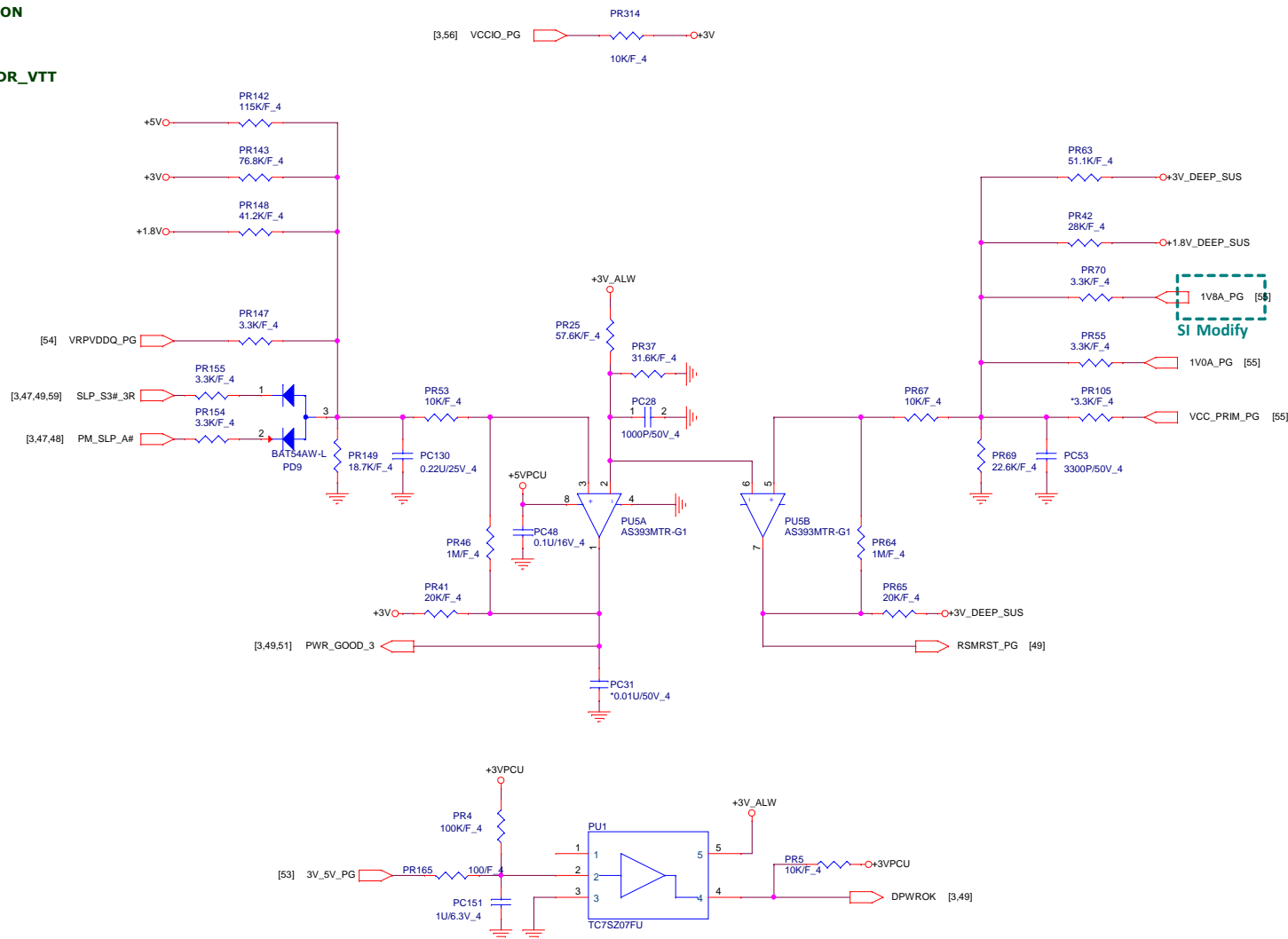
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Custom	60 -- +1.0V_VGA/1.8V_VGA/3V_VGA	1A
Date: Thursday, May 19, 2016	Sheet 61 of 67	

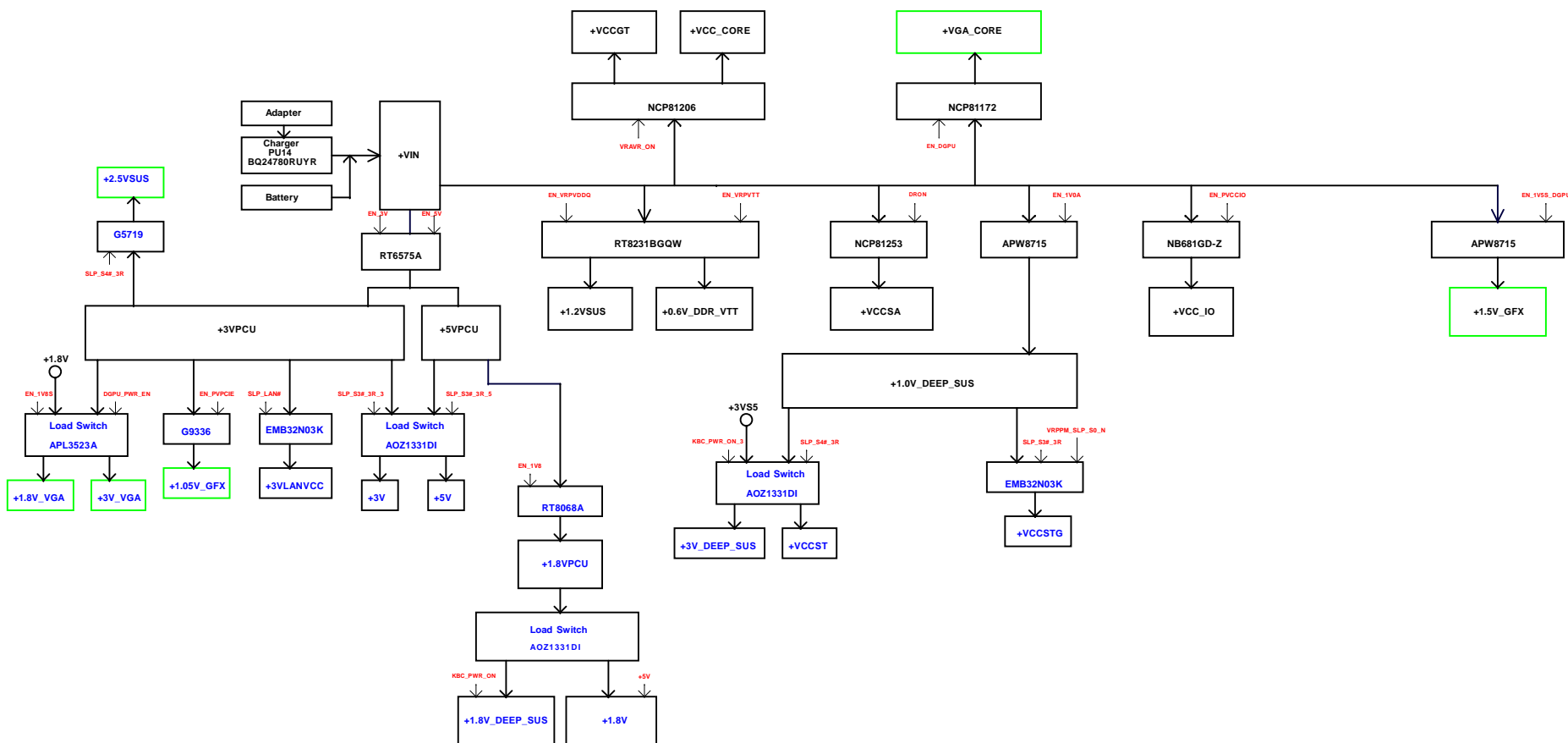


Adapter OCP

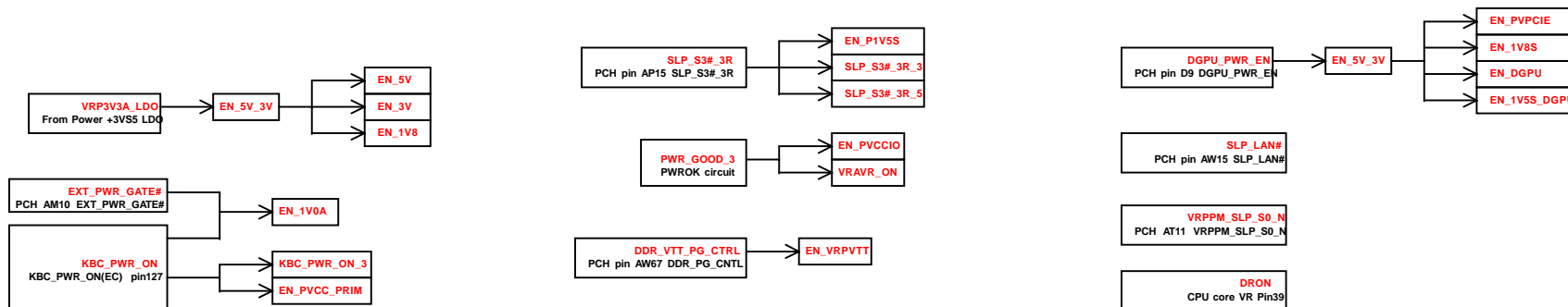


```
PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S = +0.75V_DDR_VTT
```



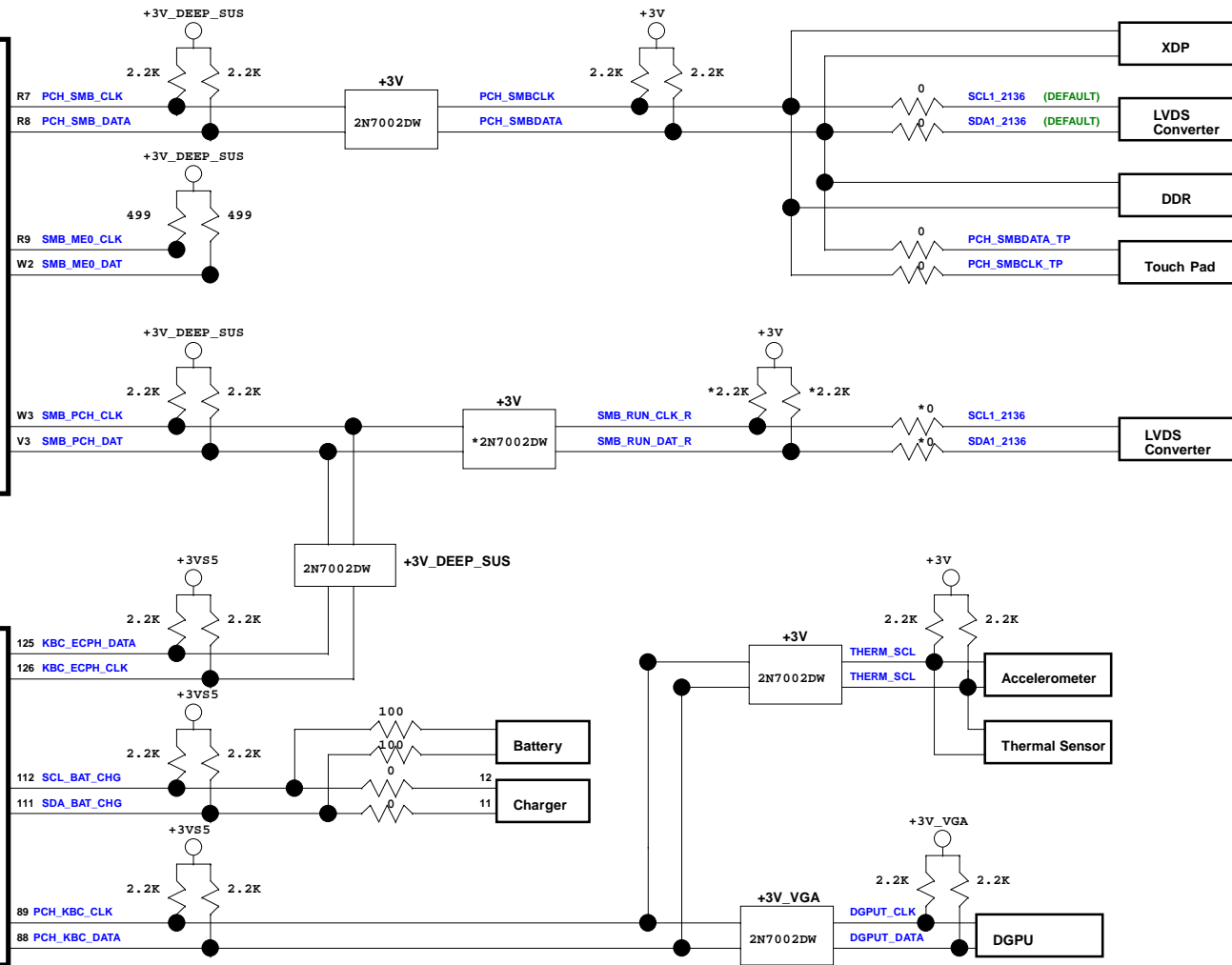


POWER ENABLE PIN



SKYLAKE U

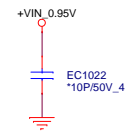
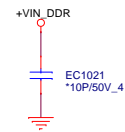
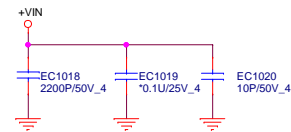
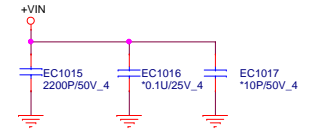
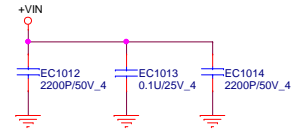
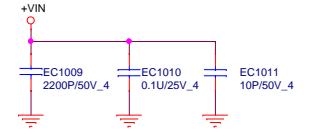
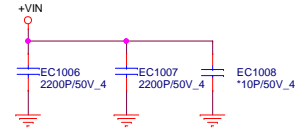
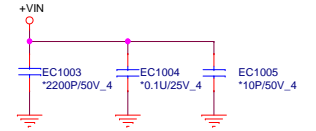
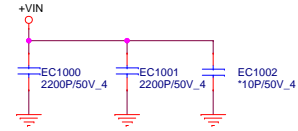
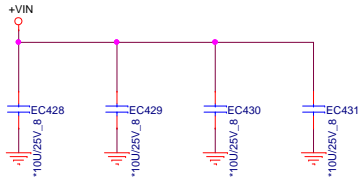
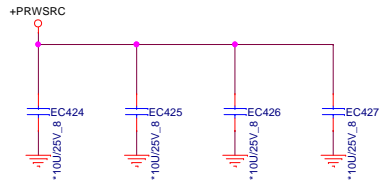
EC
NPCE586H



Example: *499/F_4 and *0_6/S
 * means none-installed
 499 means value
 F means 1%
 _4 means 0402 size
 /S means short pad

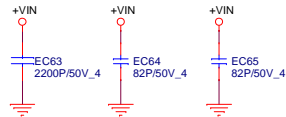
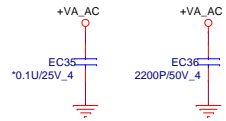
Mult i plexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Lef t s i de do wn)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Lef t s i de up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Lef t s i de do wn)
USB2 #2	USB2.0/USB3.0 Combo Jack(Lef t s i de up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC

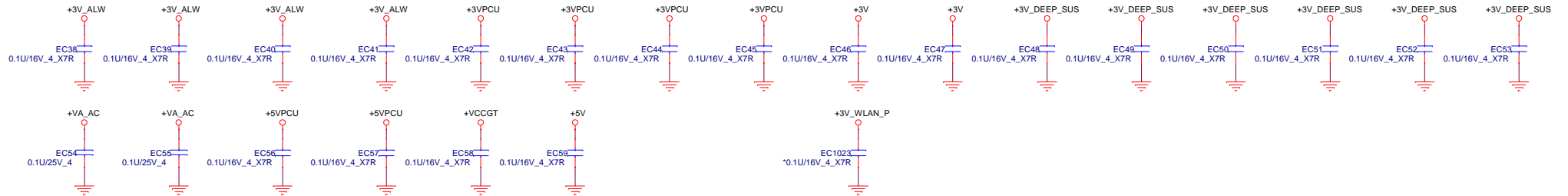


EMI cap

RF cap



EMI cap



Title			
<Title>			
Size	Document	Number	Rev
Custom	Doc		<Rev>
Date:	Thursday, May 19, 2016		
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